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# An HF Vector Network Analyzer – Part 2

*You can have most of the performance of the high-priced spreads at a fraction of the cost!*

This is the second part of a three-part article that describes a homebrew vector network analyzer (VNA) for transmission and reflection measurements from 0.05 to 60 MHz., with optional narrowband extensions for measurements through 500 MHz. This VNA requires an IBM compatible PC and uses custom software.

Part 1 described some measurement examples, theory of operation, and a performance summary. This part contains the schematic, PCB, construction, support circuits, and acknowledgements. Part 3 will deal with the software, general usage, and narrowband extensions to VHF and UHF.

**Hardware Overview**

The following hardware will be needed to perform basic transmission and reflection measurements:

- The VNA PCB
- A homebrew or purchased master oscillator that resides on the VNA PCB
- A power interface (board) that provides the DC voltages needed by the VNA PCB and also provides other power conditioning functions such as power-on surge protection, electrical noise attenuation, and over-voltage & over-current protection.
- Two to six 50 Ω coax cables between the VNA PCB and enclosure jacks. The number depends on the user's test requirements. SMA jacks are recommended.
- A metal enclosure to house the VNA PCB and power interface.
- A reflection bridge.
- Open, Short, Load (usually a precision 50 Ω), and a Thru line to be used as calibration standards. SMA connectors are recommended for calibration standards.
- (SMA) connectors to mount discrete component DUTs (Device Under Test) for reflection measurements.
- Miscellaneous (SMA) 50 Ω cables to connect a variety of DUTs to the VNA. (Surplus semi-rigid SMA coax cable assemblies are useful.)

In addition, the following hardware can be useful for certain types of more specialized testing:

- A selection of (SMA) fixed attenuators ranging from 0 to 20 dB. Fixed attenuators are useful for limiting inputs to the linear region of non-linear DUTs. 0 dB attenuators are useful to provide mechanical matching to other attenuators in use.
- A step attenuator is useful to quickly set a desired level.
- Coaxial adapters to permit testing devices with connectors other than SMA.
- An RF DDS buffer. It is a nominal overall 0 dB gain block with an output attenuator. Its primary function is to improve the source return loss below 200 kHz and above 40 MHz. This mainly benefits transmission measurement accuracy, and does next to nothing for reflection measurement accuracy. This buffer can also be useful in protecting the RF DDS from accidental damage. However, since it does have higher output harmonic levels and greater variability of output level with temperature, its routine use is not recommended.
- A Detector RF In pre-amplifier. It is a nominal overall 21 dB block with an input attenuator. Its primary functions are to bring low levels signals out of the noise floor while also providing a good input return loss. This amplifier, since it does have gain, can improve reflection and transmission measurement accuracy, particularly in those instances where the signal to the DUT has been attenuated to maintain linearity. It can also be useful in protecting the Detector from accidental damage. However, since it does have higher output harmonic levels and greater variability of output level with temperature, its routine use is not recommended.
- Power splitters, combiners, and step attenuators for ancillary uses of the VNA for things like MDS and IP3 testing.

Most of the above hardware will be described, essentially in order, in this Part. The rest will be described in Part 3 along with some ancillary test options and other add-ons that permit narrowband (2m, 70 cm, etc) extensions for reflection measurements (and possibly transmission) to over 500 MHz.

**'Build Info' Files**

In addition to the schematics and parts lists for all major hardware functions included below, 'build info' ZIP files are available at the website that expand on what is presented here. 'Build info' files are useful for builders but generally contain more information than is likely to be of interest to the casual reader.

A typical 'build info' file will contain an ExpressPCB [1] compatible artwork PCB file and a PDF file. The PCB file can be used to either purchase the main VNA board or homebrew etch the support hardware boards as needed. The PDF file will generally contain:

- Each PCB layer, expanded to full page, to permit easy identification of component locations and land patterns. These pages can be stapled together in order for x-ray views of the printed circuit board and its components. 'Virtual' silkscreens are provided as none are present on either homebrew etched boards or the Mini-board from ExpressPCB.
- Photograph(s) of the populated boards

The info contained in the 'build info' files along with the schematics and parts list included here will hopefully be sufficient for successful replication by a reasonably skilled experimenter/homebrewer with surface mount experience.

**Main VNA Board**

The schematics for the VNA printed circuit board are on Figures 1 and 2. The parts list is on Figure 3, and a 'build info' ZIP file is available at the website [2]. The schematics also show some key DC voltages to aid the builder in initial bring-up and debug.

Circuit Overview

The description here is intended to augment the "Theory of Operation" and the "Performance Summary" sections in Part 1. Those sections and the VNA block diagram shown in Figure 16 of Part 1 should be referred to as needed. The references also contain URLs for many of the components.

Figure 1 contains:

- The interface between the PC parallel port and VNA programmable functions.
- The master oscillator.
- A pair of direct digital synthesis (DDS) signal sources.
- Two anti-alias filters.
- An optional master oscillator test point.
- +5V Power Interface

PC Interface

J160, U160, Q190, and some RC components provide an electrically compatible interface to an IEEE 1284 PC parallel port. These components, in particular the 74ACT1284 [3], provide buffering and protection for the remaining circuitry against accidental short circuits and certain over-voltage conditions. The buffering also provides approximately 0.5V hysteresis and RC filter networks for improved noise immunity.

**The use of an IEEE 1284 compatible external cable is recommended to ensure adequate impedance control and noise immunity. It is possible that some (poor) parallel cables that do not meet IEEE 1284 will cause software mal-functions.**

Individual VNA hardware lines are mated, with a few exceptions, to individual PC parallel port lines. This type of control:

- Puts all the intelligence needed to program the VNA in PC software,
- Eliminates the need for a micro-controller at the VNA end, and
- Allows the greatest flexibility in hardware control & ease of software updates.

Providing common control functions was done in a few cases where either there was no perceived need for independent control or it was necessary to obtain certain desired functions. A secondary goal was to have as many parallel port I/Os as possible available for future expansion.

The level of hardware 'bit twiddling' required here is interfered with in some PC operating systems, notably Windows 2000 and XP. However, there are workarounds available for those two that permit proper VNA operation.

Master Oscillator

The U140 master oscillator operates at a nominal 148.344 MHz. It provides the clock to the U110 and U120 DDS modules and also synchronizes the DDS FQ_UD line as received from the PC via double latching in U130, the 74AC74 D-type flip-flop [4]. In this application, each stage of the flip-flop is used as a data latch, basically recording the state of its input at the time the rising clock edge occurs. The output of the first stage feeds the input of the second stage. The output of the second stage is used by the DDSs. This 'double latching' is a useful technique to reduce the probability of metastability [5]. This synchronization ensures that the two DDSs maintain the desired relative phase for essentially all [6] frequency programming performed.

As indicated in Part 1, the master oscillator frequency was chosen to prevent a slight increase of noise in the measured data from occurring at round number test frequencies, which are generally the most likely to be used. It also happened to be the $7^{th}$ overtone frequency of an on-hand $5^{th}$ overtone crystal! The measured data noise increases are due to DDS inverted alias spurs that occur for DDS output frequencies near the clock frequency divided by an integer - most notably, three. Part 3 will contain test results to show that the noise in the measured data at Fclk/3, or about 49.45 MHz, affects a typical impedance measurement only slightly. Data at lower integer divisor frequencies have even less noise.

There are options in the parts list to either homebrew the master oscillator or purchase a packaged one. The homebrew master oscillator and a test board that can be used for homebrew or packaged oscillators will be described in greater detail in a subsequent section.

Packaged Master Oscillator

As indicated in the parts list, the only tested U140 alt. option is the Valpey-Fisher unit. This unit was at 148 MHz, since it was a stocked frequency. It was found to offer near-in phase noise performance comparable to the homebrew master oscillator, but a slightly worse temperature coefficient of -0.15 ppm/°C vs. -0.10 ppm/°C for a homebrew master oscillator. The initial warm-up (power-on) drift for the Valpey-Fisher unit was –1.2 ppm vs. -3.2 ppm for the homebrew master oscillator.

Generally, the U140 alt. options are offered for those that do not want to homebrew the master oscillator. The Fox part numbers have not been tested, and are suggested only as *possible* candidates. They use internal PLLs and will have more jitter and phase noise than the homebrew master oscillator or the Valpey-Fisher unit, which does not have an internal PLL The Valpey-Fisher unit is spec'd for 1 ps jitter, while the Fox units are on the order of 20 ps [7]

Master oscillator phase noise & jitter is expected to be more important to ancillary uses of the VNA hardware, such as IP3 testing, and less significant to conventional VNA testing as long as the DDS PLLs are not enabled.

The master oscillator clocks both DDSs at the same times, every 6.74 ns approximately, in essentially lock-step fashion with the same jitter applied to both DDS outputs. Conventional VNA testing depends on relative phase, and relative phase between the two DDSs is preserved, given the various operative time constants generally encountered. The only exception that I can imagine would be a test of an extremely narrowband filter. Even that seems unlikely given the 5 Hz detector bandwidth.

If of interest to a prospective builder, the Fox unit should first be tested for functionality in the master oscillator test board. If it works there, then put it on the VNA PCB and test it for warm-up frequency drift, frequency dependency on room ambient temperature, and phase noise. Then, test the narrowest band device that might be of interest.

Master Oscillator Frequency

All VNA software programs use a 'configuration' file that defines parameters that are determined by the actual hardware in use. Each VNA user can readily edit that file to adjust the various parameters, including the master oscillator frequency. This tuning via software eliminates the need for a either a close tolerance on the master oscillator frequency or an adjustable component. This configuration file will be described in more detail in Part 3.

DDS Signal Sources

The RF DDS, U110, and the LO DDS, U120, are the Analog Devices AD9851 [8]. The DDSs are programmed using the serial load format to conserve PC parallel port I/Os. As noted in Part 1, the DDSs are independently PC programmable for both frequency and phase. While not required for the normal VNA functions, this flexibility permits other ancillary uses of the VNA, including verification of the detector phase accuracy as described below in the Detector section.

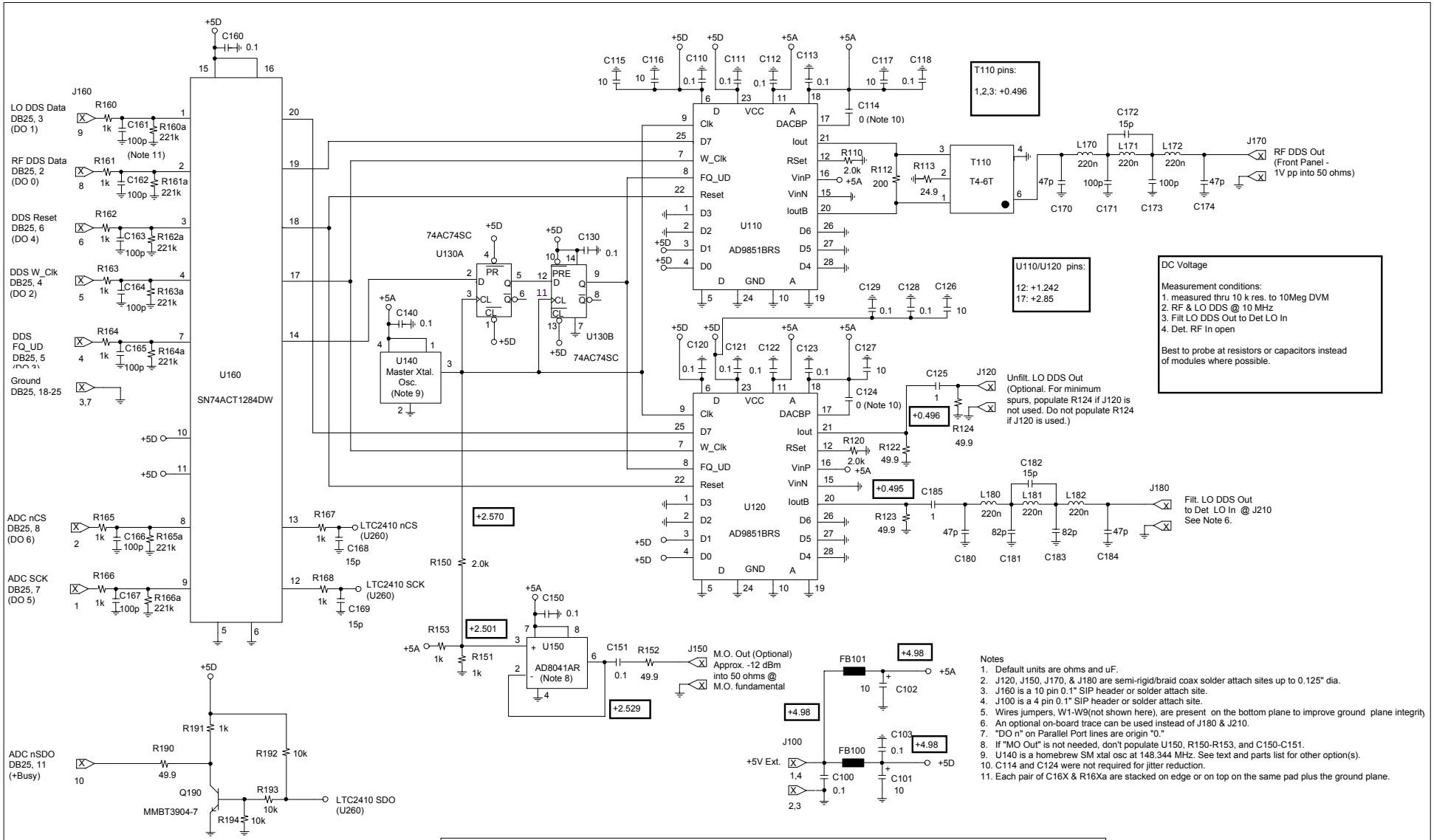



Figure 1. N2PK VNA PCB Schematic - DDS Sources

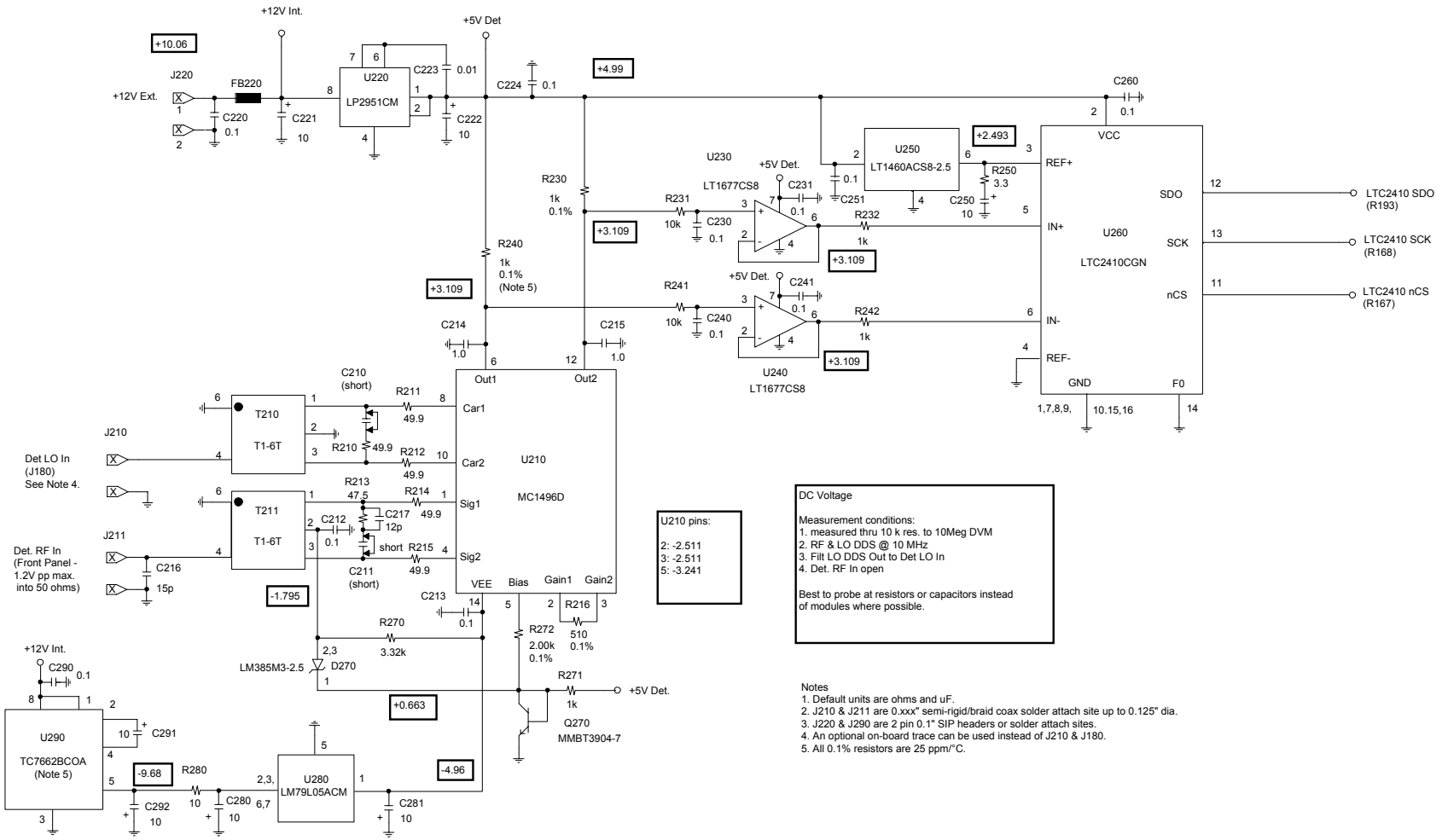



Figure 2. N2PK VNA PCB Schematic - Detector

## Figure 3. VNA PCB Parts List

| Desig. | Description | Package | Manufacturer | Mfg P/N | Vendor | Vendor P/N |
|---|---|---|---|---|---|---|
| C100 | 0.1 uF/50V/X7R/10% | 0805 | Panasonic | ECJ-2YBH104K | Digi-Key | PCC1840CT-ND |
| C101 | 10 uF/16V/Tant/20% | EIA B | Panasonic | ECS-T1CX106R | Digi-Key | PCS3106CT-ND |
| C102 | 10 uF/16V/Tant/20% | EIA B | Panasonic | ECS-T1CX106R | Digi-Key | PCS3106CT-ND |
| C103 | 0.1 uF/50V/X7R/10% | 0805 | Panasonic | ECJ-2YBH104K | Digi-Key | PCC1840CT-ND |
| C110 | 0.1 uF/50V/X7R/10% | 0805 | Panasonic | ECJ-2YBH104K | Digi-Key | PCC1840CT-ND |
| C111 | 0.1 uF/50V/X7R/10% | 0805 | Panasonic | ECJ-2YBH104K | Digi-Key | PCC1840CT-ND |
| C112 | 0.1 uF/50V/X7R/10% | 0805 | Panasonic | ECJ-2YBH104K | Digi-Key | PCC1840CT-ND |
| C113 | 0.1 uF/50V/X7R/10% | 0805 | Panasonic | ECJ-2YBH104K | Digi-Key | PCC1840CT-ND |
| C114 | 0 - not used | 1206 | | | | |
| C115 | 10 uF/16V/X5R/10% | 1210 | Panasonic | ECJ-4YB1C106K | Digi-Key | PCC2169CT-ND |
| C116 | 10 uF/16V/X5R/10% | 1210 | Panasonic | ECJ-4YB1C106K | Digi-Key | PCC2169CT-ND |
| C117 | 10 uF/16V/X5R/10% | 1210 | Panasonic | ECJ-4YB1C106K | Digi-Key | PCC2169CT-ND |
| C118 | 0.1 uF/50V/X7R/10% | 0805 | Panasonic | ECJ-2YBH104K | Digi-Key | PCC1840CT-ND |
| C120 | 0.1 uF/50V/X7R/10% | 0805 | Panasonic | ECJ-2YBH104K | Digi-Key | PCC1840CT-ND |
| C121 | 0.1 uF/50V/X7R/10% | 0805 | Panasonic | ECJ-2YBH104K | Digi-Key | PCC1840CT-ND |
| C122 | 0.1 uF/50V/X7R/10% | 0805 | Panasonic | ECJ-2YBH104K | Digi-Key | PCC1840CT-ND |
| C123 | 0.1 uF/50V/X7R/10% | 0805 | Panasonic | ECJ-2YBH104K | Digi-Key | PCC1840CT-ND |
| C124 | 0 - not used | 1206 | | | | |
| C125 | 1 uF/25V/X7R/10% | 1206 | Panasonic | ECJ-3YB1E105K | Digi-Key | PCC1893CT-ND |
| C126 | 10 uF/16V/X5R/10% | 1210 | Panasonic | ECJ-4YB1C106K | Digi-Key | PCC2169CT-ND |
| C127 | 10 uF/16V/X5R/10% | 1210 | Panasonic | ECJ-4YB1C106K | Digi-Key | PCC2169CT-ND |
| C128 | 0.1 uF/50V/X7R/10% | 0805 | Panasonic | ECJ-2YBH104K | Digi-Key | PCC1840CT-ND |
| C129 | 0.1 uF/50V/X7R/10% | 0805 | Panasonic | ECJ-2YBH104K | Digi-Key | PCC1840CT-ND |
| C130 | 0.1 uF/50V/X7R/10% | 0805 | Panasonic | ECJ-2YBH104K | Digi-Key | PCC1840CT-ND |
| C140 | 0.1 uF/50V/X7R/10% | 0805 | Panasonic | ECJ-2YBH104K | Digi-Key | PCC1840CT-ND |
| C150* | 0.1 uF/50V/X7R/10% | 0805 | Panasonic | ECJ-2YBH104K | Digi-Key | PCC1840CT-ND |
| C151* | 0.1 uF/50V/X7R/10% | 0805 | Panasonic | ECJ-2YBH104K | Digi-Key | PCC1840CT-ND |
| C160 | 0.1 uF/50V/X7R/10% | 0805 | Panasonic | ECJ-2YBH104K | Digi-Key | PCC1840CT-ND |
| C161 | 100 pF/50V/NPO/5% | 0805 | Panasonic | ECJ-2VC1H101J | Digi-Key | PCC101CGCT-ND |
| C162 | 100 pF/50V/NPO/5% | 0805 | Panasonic | ECJ-2VC1H101J | Digi-Key | PCC101CGCT-ND |
| C163 | 100 pF/50V/NPO/5% | 0805 | Panasonic | ECJ-2VC1H101J | Digi-Key | PCC101CGCT-ND |
| C164 | 100 pF/50V/NPO/5% | 0805 | Panasonic | ECJ-2VC1H101J | Digi-Key | PCC101CGCT-ND |
| C165 | 100 pF/50V/NPO/5% | 0805 | Panasonic | ECJ-2VC1H101J | Digi-Key | PCC101CGCT-ND |
| C166 | 100 pF/50V/NPO/5% | 0805 | Panasonic | ECJ-2VC1H101J | Digi-Key | PCC101CGCT-ND |
| C167 | 100 pF/50V/NPO/5% | 0805 | Panasonic | ECJ-2VC1H101J | Digi-Key | PCC101CGCT-ND |
| C168 | 15 pF/50V/NPO/5% | 0805 | Panasonic | ECJ-2VC1H150J | Digi-Key | PCC150CNCT-ND |
| C169 | 15 pF/50V/NPO/5% | 0805 | Panasonic | ECJ-2VC1H150J | Digi-Key | PCC150CNCT-ND |
| C170 | 47 pF/50V/NPO/5% | 0805 | Panasonic | ECJ-2VC1H470J | Digi-Key | PCC470CGCT-ND |
| C171 | 100 pF/50V/NPO/5% | 0805 | Panasonic | ECJ-2VC1H101J | Digi-Key | PCC101CGCT-ND |
| C172 | 15 pF/50V/NPO/5% | 0805 | Panasonic | ECJ-2VC1H150J | Digi-Key | PCC150CNCT-ND |
| C173 | 100 pF/50V/NPO/5% | 0805 | Panasonic | ECJ-2VC1H101J | Digi-Key | PCC101CGCT-ND |
| C174 | 47 pF/50V/NPO/5% | 0805 | Panasonic | ECJ-2VC1H470J | Digi-Key | PCC470CGCT-ND |
| C180 | 47 pF/50V/NPO/5% | 0805 | Panasonic | ECJ-2VC1H470J | Digi-Key | PCC470CGCT-ND |
| C181 | 82 pF/50V/NPO/5% | 0805 | Panasonic | ECJ-2VC1H820J | Digi-Key | PCC820CGCT-ND |
| C182 | 15 pF/50V/NPO/5% | 0805 | Panasonic | ECJ-2VC1H150J | Digi-Key | PCC150CNCT-ND |
| C183 | 82 pF/50V/NPO/5% | 0805 | Panasonic | ECJ-2VC1H820J | Digi-Key | PCC820CGCT-ND |
| C184 | 47 pF/50V/NPO/5% | 0805 | Panasonic | ECJ-2VC1H470J | Digi-Key | PCC470CGCT-ND |
| C185 | 1 uF/25V/X7R/10% | 1206 | Panasonic | ECJ-3YB1E105K | Digi-Key | PCC1893CT-ND |
| C210 | replaced by a short | 0805 | | | | |
| C211 | replaced by a short | 0805 | | | | |
| C212 | 0.1 uF/50V/X7R/10% | 0805 | Panasonic | ECJ-2YBH104K | Digi-Key | PCC1840CT-ND |
| C213 | 0.1 uF/50V/X7R/10% | 0805 | Panasonic | ECJ-2YBH104K | Digi-Key | PCC1840CT-ND |
| C214 | 1 uF/25V/X7R/10% | 1206 | Panasonic | ECJ-3YB1E105K | Digi-Key | PCC1893CT-ND |
| C215 | 1 uF/25V/X7R/10% | 1206 | Panasonic | ECJ-3YB1E105K | Digi-Key | PCC1893CT-ND |
| C216 | 15 pF/50V/NPO/5% | 0805 | Panasonic | ECJ-2VC1H150J | Digi-Key | PCC150CNCT-ND |
| C217 | 12 pF/50V/NPO/5% | 0805 | Panasonic | ECJ-2VC1H120J | Digi-Key | PCC120CNCT-ND |
| C220 | 0.1 uF/50V/X7R/10% | 0805 | Panasonic | ECJ-2YBH104K | Digi-Key | PCC1840CT-ND |
| C221 | 10 uF/16V/Tant/20% | EIA B | Panasonic | ECS-T1CX106R | Digi-Key | PCS3106CT-ND |
| C222 | 10 uF/16V/Tant/20% | EIA B | Panasonic | ECS-T1CX106R | Digi-Key | PCS3106CT-ND |
| C223 | 0.01 uF/50V/X7R/10% | 0805 | Panasonic | ECJ-2VB1H103K | Digi-Key | PCC103BNCT-ND |

## Figure 3. VNA PCB Parts List

| Desig. | Description | Package | Manufacturer | Mfg P/N | Vendor | Vendor P/N |
|---|---|---|---|---|---|---|
| C224 | 0.1 uF/50V/X7R/10% | 0805 | Panasonic | ECJ-2YBH104K | Digi-Key | PCC1840CT-ND |
| C230 | 0.1 uF/50V/X7R/10% | 0805 | Panasonic | ECJ-2YBH104K | Digi-Key | PCC1840CT-ND |
| C231 | 0.1 uF/50V/X7R/10% | 0805 | Panasonic | ECJ-2YBH104K | Digi-Key | PCC1840CT-ND |
| C240 | 0.1 uF/50V/X7R/10% | 0805 | Panasonic | ECJ-2YBH104K | Digi-Key | PCC1840CT-ND |
| C241 | 0.1 uF/50V/X7R/10% | 0805 | Panasonic | ECJ-2YBH104K | Digi-Key | PCC1840CT-ND |
| C250 | 10 uF/16V/Tant/20% | EIA B | Panasonic | ECS-T1CX106R | Digi-Key | PCS3106CT-ND |
| C251 | 0.1 uF/50V/X7R/10% | 0805 | Panasonic | ECJ-2YBH104K | Digi-Key | PCC1840CT-ND |
| C260 | 0.1 uF/50V/X7R/10% | 0805 | Panasonic | ECJ-2YBH104K | Digi-Key | PCC1840CT-ND |
| C280 | 10 uF/16V/Tant/20% | EIA B | Panasonic | ECS-T1CX106R | Digi-Key | PCS3106CT-ND |
| C281 | 10 uF/16V/Tant/20% | EIA B | Panasonic | ECS-T1CX106R | Digi-Key | PCS3106CT-ND |
| C290 | 0.1 uF/50V/X7R/10% | 0805 | Panasonic | ECJ-2YBH104K | Digi-Key | PCC1840CT-ND |
| C291 | 10 uF/16V/Tant/20% | EIA B | Panasonic | ECS-T1CX106R | Digi-Key | PCS3106CT-ND |
| C292 | 10 uF/16V/Tant/20% | EIA B | Panasonic | ECS-T1CX106R | Digi-Key | PCS3106CT-ND |
| D270 | Voltage Ref. Diode | SOT-23 | Nat'l | LM385M3-2.5 | Digi-Key | LM385M3-2.5CT-ND |
| FB100 | Ferrite Bead | 1806 | Panasonic | EXC-ML45A910H | Digi-Key | P11956CT-ND |
| FB101 | Ferrite Bead | 1806 | Panasonic | EXC-ML45A910H | Digi-Key | P11956CT-ND |
| FB220 | Ferrite Bead | 1806 | Panasonic | EXC-ML45A910H | Digi-Key | P11956CT-ND |
| J100 | 4 Pos. Pol. Header | 0.1" SIP | Amp/Tyco | 641213-4 | Digi-Key | A23899-ND |
| J100 mate | 4 Pos. Pol. Receptacle | 0.1" SIP | Amp/Tyco | 770602-4 | Digi-Key | A19492-ND |
| J160 | 10 Pos. Pol. Header | 0.1" SIP | Amp/Tyco | 1-640454-0 | Digi-Key | A19437-ND |
| J160 mate | 10 Pos. Pol. Receptacle | 0.1" SIP | Amp/Tyco | 1-770602-0 | Digi-Key | A19498-ND |
| J220 | 2 Pos. Pol. Header | 0.1" SIP | Amp/Tyco | 641213-2 | Digi-Key | A23897-ND |
| J220 mate | 2 Pos. Pol. Receptacle | 0.1" SIP | Amp/Tyco | 770602-2 | Digi-Key | A19490-ND |
| | Gold Recept. contacts | | Amp/Tyco | 770601-2 | Digi-Key | A23963-ND |
| L170 | 0.22 uH/Shield/10% | see mfg dwg | API Delevan | S1210-221K | Digi-Key | DN1054CT-ND |
| L171 | 0.22 uH/Shield/10% | see mfg dwg | API Delevan | S1210-221K | Digi-Key | DN1054CT-ND |
| L172 | 0.22 uH/Shield/10% | see mfg dwg | API Delevan | S1210-221K | Digi-Key | DN1054CT-ND |
| L180 | 0.22 uH/Shield/10% | see mfg dwg | API Delevan | S1210-221K | Digi-Key | DN1054CT-ND |
| L181 | 0.22 uH/Shield/10% | see mfg dwg | API Delevan | S1210-221K | Digi-Key | DN1054CT-ND |
| L182 | 0.22 uH/Shield/10% | see mfg dwg | API Delevan | S1210-221K | Digi-Key | DN1054CT-ND |
| PCB | Printed Ckt Board | see file | Express PCB | Miniboard | Exp. PCB | file: VNAV1A.PCB |
| Q190 | NPN tx | SOT-23 | Diodes Inc. | MMBT3904-7 | Digi-Key | MMBT3904DICT-ND |
| Q270 | NPN Tx | SOT-23 | Diodes Inc. | MMBT3904-7 | Digi-Key | MMBT3904DICT-ND |
| R110 | 2.00K/0.1w/1% | 0805 | Panasonic | ERJ-6ENF2001V | Digi-Key | P2.00KCCT-ND |
| R112 | 200/0.1w/1% | 0805 | Panasonic | ERJ-6ENF2000V | Digi-Key | P200CCT-ND |
| R113 | 24.9/0.1w/1% | 0805 | Panasonic | ERJ-6ENF24R9V | Digi-Key | P24.9CCT-ND |
| R120 | 2.00K/0.1w/1% | 0805 | Panasonic | ERJ-6ENF2001V | Digi-Key | P2.00KCCT-ND |
| R122 | 49.9/0.1w/1% | 0805 | Panasonic | ERJ-6ENF49R9V | Digi-Key | P49.9CCT-ND |
| R123 | 49.9/0.1w/1% | 0805 | Panasonic | ERJ-6ENF49R9V | Digi-Key | P49.9CCT-ND |
| R124** | 49.9/0.1w/1% | 0805 | Panasonic | ERJ-6ENF49R9V | Digi-Key | P49.9CCT-ND |
| R150* | 2.00K/0.1w/1% | 0805 | Panasonic | ERJ-6ENF2001V | Digi-Key | P2.00KCCT-ND |
| R151* | 1.00K/0.1w/1% | 0805 | Panasonic | ERJ-6ENF1001V | Digi-Key | P1.00KCCT-ND |
| R152* | 49.9/0.1w/1% | 0805 | Panasonic | ERJ-6ENF49R9V | Digi-Key | P49.9CCT-ND |
| R153* | 1.00K/0.1w/1% | 0805 | Panasonic | ERJ-6ENF1001V | Digi-Key | P1.00KCCT-ND |
| R160 | 1.00K/0.1w/1% | 0805 | Panasonic | ERJ-6ENF1001V | Digi-Key | P1.00KCCT-ND |
| R160a | 221k/0.1w/1% | 0805 | Panasonic | ERJ-6ENF2213V | Digi-Key | P221KCCT-ND |
| R161 | 1.00K/0.1w/1% | 0805 | Panasonic | ERJ-6ENF1001V | Digi-Key | P1.00KCCT-ND |
| R161a | 221k/0.1w/1% | 0805 | Panasonic | ERJ-6ENF2213V | Digi-Key | P221KCCT-ND |
| R162 | 1.00K/0.1w/1% | 0805 | Panasonic | ERJ-6ENF1001V | Digi-Key | P1.00KCCT-ND |
| R162a | 221k/0.1w/1% | 0805 | Panasonic | ERJ-6ENF2213V | Digi-Key | P221KCCT-ND |
| R163 | 1.00K/0.1w/1% | 0805 | Panasonic | ERJ-6ENF1001V | Digi-Key | P1.00KCCT-ND |
| R163a | 221k/0.1w/1% | 0805 | Panasonic | ERJ-6ENF2213V | Digi-Key | P221KCCT-ND |
| R164 | 1.00K/0.1w/1% | 0805 | Panasonic | ERJ-6ENF1001V | Digi-Key | P1.00KCCT-ND |
| R164a | 221k/0.1w/1% | 0805 | Panasonic | ERJ-6ENF2213V | Digi-Key | P221KCCT-ND |
| R165 | 1.00K/0.1w/1% | 0805 | Panasonic | ERJ-6ENF1001V | Digi-Key | P1.00KCCT-ND |
| R165a | 221k/0.1w/1% | 0805 | Panasonic | ERJ-6ENF2213V | Digi-Key | P221KCCT-ND |
| R166 | 1.00K/0.1w/1% | 0805 | Panasonic | ERJ-6ENF1001V | Digi-Key | P1.00KCCT-ND |
| R166a | 221k/0.1w/1% | 0805 | Panasonic | ERJ-6ENF2213V | Digi-Key | P221KCCT-ND |
| R167 | 1.00K/0.1w/1% | 0805 | Panasonic | ERJ-6ENF1001V | Digi-Key | P1.00KCCT-ND |
| R168 | 1.00K/0.1w/1% | 0805 | Panasonic | ERJ-6ENF1001V | Digi-Key | P1.00KCCT-ND |

## Figure 3. VNA PCB Parts List

| Desig. | Description | Package | Manufacturer | Mfg P/N | Vendor | Vendor P/N |
|---|---|---|---|---|---|---|
| R190 | 49.9/0.1w/1% | 0805 | Panasonic | ERJ-6ENF49R9V | Digi-Key | P49.9CCT-ND |
| R191 | 1.00K/0.1w/1% | 0805 | Panasonic | ERJ-6ENF1001V | Digi-Key | P1.00KCCT-ND |
| R192 | 10.0K/0.1w/1% | 0805 | Panasonic | ERJ-6ENF1002V | Digi-Key | P10.0KCCT-ND |
| R193 | 10.0K/0.1w/1% | 0805 | Panasonic | ERJ-6ENF1002V | Digi-Key | P10.0KCCT-ND |
| R194 | 10.0K/0.1w/1% | 0805 | Panasonic | ERJ-6ENF1002V | Digi-Key | P10.0KCCT-ND |
| R210 | 49.9/0.1w/1% | 0805 | Panasonic | ERJ-6ENF49R9V | Digi-Key | P49.9CCT-ND |
| R211 | 49.9/0.1w/1% | 0805 | Panasonic | ERJ-6ENF49R9V | Digi-Key | P49.9CCT-ND |
| R212 | 49.9/0.1w/1% | 0805 | Panasonic | ERJ-6ENF49R9V | Digi-Key | P49.9CCT-ND |
| R213 | 47.5/0.1w/1% | 0805 | Panasonic | ERJ-6ENF47R5V | Digi-Key | P47.5CCT-ND |
| R214 | 49.9/0.1w/1% | 0805 | Panasonic | ERJ-6ENF49R9V | Digi-Key | P49.9CCT-ND |
| R215 | 49.9/0.1w/1% | 0805 | Panasonic | ERJ-6ENF49R9V | Digi-Key | P49.9CCT-ND |
| R216 | 510/0.1w/0.1% | 0805 | Panasonic | ERA-6YEB511V | Digi-Key | P510ZCT-ND |
| R230 | 1.00K/0.1w/0.1% | 0805 | Panasonic | ERA-6YEB102V | Digi-Key | P1.0KZCT-ND |
| R231 | 10.0K/0.1w/1% | 0805 | Panasonic | ERJ-6ENF1002V | Digi-Key | P10.0KCCT-ND |
| R232 | 1.00K/0.1w/1% | 0805 | Panasonic | ERJ-6ENF1001V | Digi-Key | P1.00KCCT-ND |
| R240 | 1.00K/0.1w/0.1% | 0805 | Panasonic | ERA-6YEB102V | Digi-Key | P1.0KZCT-ND |
| R241 | 10.0K/0.1w/1% | 0805 | Panasonic | ERJ-6ENF1002V | Digi-Key | P10.0KCCT-ND |
| R242 | 1.00K/0.1w/1% | 0805 | Panasonic | ERJ-6ENF1001V | Digi-Key | P1.00KCCT-ND |
| R250 | 3.3/0.1w/5% | 0805 | Panasonic | ERJ-6GEYJ3R3V | Digi-Key | P3.3ACT-ND |
| R270 | 3.32K/0.1w/1% | 0805 | Panasonic | ERJ-6ENF3321V | Digi-Key | P3.32KCCT-ND |
| R271 | 1.00K/0.1w/1% | 0805 | Panasonic | ERJ-6ENF1001V | Digi-Key | P1.00KCCT-ND |
| R272 | 2.00K/0.1w/0.1% | 0805 | Panasonic | ERA-6YEB202V | Digi-Key | P2.0KZCT-ND |
| R280 | 10.0/0.1w/1% | 0805 | Panasonic | ERJ-6ENF10R0V | Digi-Key | P10.0CCT-ND |
| T110 | 2CT:1 T.R. Xfmr | KK81 | Mini-Ckt | T4-6T-KK81 | Mini-Ckt | T4-6T-KK81 |
| T210 | 1:1CT T.R. Xfmr | KK81 | Mini-Ckt | T1-6T-KK81 | Mini-Ckt | T1-6T-KK81 |
| T211 | 1:1CT T.R. Xfmr | KK81 | Mini-Ckt | T1-6T-KK81 | Mini-Ckt | T1-6T-KK81 |
| U110 | DDS | SSOP-28 | ADI | AD9851BRS | Arrow | AD9851BRS |
| U120 | DDS | SSOP-28 | ADI | AD9851BRS | Arrow | AD9851BRS |
| U130 | Dual D Flip-Flop | SO-14 | Fairchild | 74AC74SC | Digi-Key | 74AC74SC-ND |
| U140 | 148.344 MHz Xtal Osc. | see text | homebrew | see text | | |
| U140 alt. | 148.344MHz Pkg'd Osc | SOJ | Valpey | see notes & text | Valpey | see notes & text |
| U140 alt. | 148.344MHz Pkg'd Osc | SOJ | Fox | see notes & text | Mouser | see notes & text |
| U150* | Amplifier | SO-8 | ADI | AD8041AR | Arrow | AD8041AR |
| U160 | 7 Bit Bus Interface | SO-20 | TI | SN74ACT1284DW | Digi-Key | 296-1067-5-ND |
| U210 | Bal.Demodulator | SO-14 | Mot/Nat'l | MC1496D/LM1496M | Arrow | MC1496D |
| U220 | +1.2-29V Lin. Reg | SO-8 | Nat'l | LP2951CM | Digi-Key | LP2951CM-ND |
| U230 | Low Noise Op Amp | SO-8 | Lin Tech | LT1677CS8 | Arrow | LT1677CS8 |
| U240 | Low Noise Op Amp | SO-8 | Lin Tech | LT1677CS8 | Arrow | LT1677CS8 |
| U250 | Precision 2.5V Ref. | SO-8 | Lin Tech | LT1460ACS8-2.5 | Arrow | LT1460ACS8-2.5 |
| U260 | 24 Bit ADC | SSOP-16 | Lin Tech | LTC2410CGN | Arrow | LTC2410CGN |
| U280 | -5V Voltage Reg. | SO-8 | Nat'l | LM79L05ACM | Digi-Key | LM79L05ACM-ND |
| U290 | DC-DC Volt. Conv. | SO-8 | Microchip | TC7662BCOA | Digi-Key | 158-1066-ND |

* optional - not needed if "M.O. Out" at J150 is not used. "M.O. Out" can also be used without U150 - see text.

** don't use if J120 is used.

NOTE: The only tested U140 alt is the Valpey-Fisher unit (@ 148 MHz). The Fox unit is untested, but will have higher jitter.

Legend/URLs:

| | |
|---|---|
| ADI - Analog Devices Inc, | http://www.analog.com/index.html |
| Amp/Tyco - | http://www.amp.com/ |
| API Delevan - | http://www.delevan.com/PDF_DOCS/S1210.pdf |
| Arrow - Arrow Electronics, | http://www.arrow.com |
| Digi-key - | http://www.digikey.com/ |
| Exp PCB - ExpressPCB, | http://www.expresspcb.com/ |
| Fox - JITO-2-PC5CEC-148.344000 (untested) | http://www.foxonline.com/jito_p.htm |
| Lin Tech - Linear Technology, | http://www.linear-tech.com |
| Microchip - | http://www.microchip.com |
| Mini-Ckt - Mini-Circuits, | http://www.minicircuits.com |
| Mouser - JITO-PC5CE-148.344000 (untested) | http://www.mouser.com/ |
| Valpey-Fisher - VFAC570BH-148.344MHz (or 148 MHz - see text) | http://www.valpeyfisher.com/ |

Parts can be obtained directly from the manufacturer in some cases.

The two DDS "Reset", W_Clk, and FQ_UD lines are controlled in common by the PC. Common "Reset" and "W_Clk" so far has not resulted in an inability to program a desired control function. Providing a common "FQ_UD" which is also synchronized to the DDS "Clk" line is required to obtain the desired phasing control. Independent control of the DDS "D7" lines provides the desired flexibility for frequency and relative phase.

With the 148.34 MHz clock rate and the 32 bit tuning word, the DDS frequency resolution is approximately 0.035 Hz.

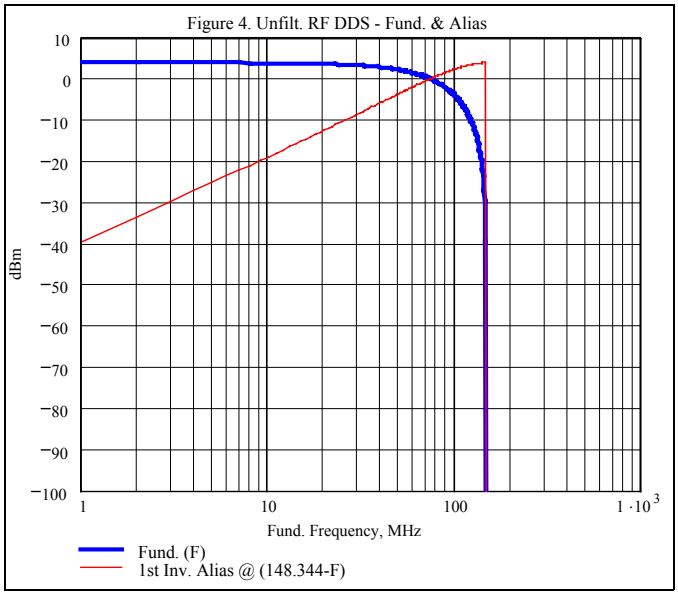
The two RF DDS outputs are combined differentially in the 2:1 turns ratio transformer T110 to obtain a 6 dB higher output and also to minimize spurious outputs. R112 provides the source match and R113 provides a DC offset to keep the voltage swings at the DDS outputs within acceptable limits. The two LO DDS outputs are each single-ended, as two individual outputs were felt to be useful and the higher amplitude was not needed for the Detector LO Input.

Anti-alias Filters

The unfiltered RF DDS output magnitudes for the fundamental at F and the 1st inverted alias, which is located at (Fclk-F), are shown in Figure 4. Fclk is the master oscillator frequency, which is nominally 148.344 MHz.

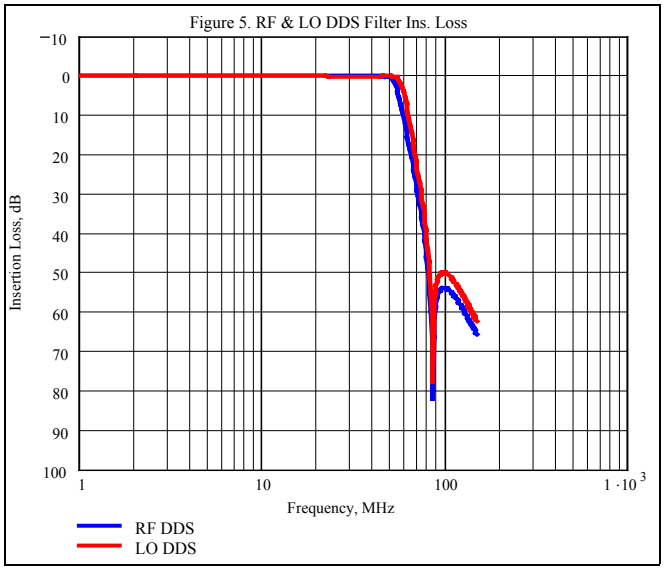
For example, if we start with a 1 MHz fundamental output, it will be at +4 dBm, then the 1st inverted alias will be at 147.344 MHz and it will be 44 dB down at –40 dBm.

As we increase the fundamental frequency, the inverted alias will decrease in frequency, approaching the fundamental, and will be growing in magnitude. At the Nyquist frequency of 74.172 MHz, the fundamental and 1st inverted alias are equal in frequency and their magnitudes are also equal at about 0 dBm. Above the Nyquist frequency, the 1st inverted alias is higher amplitude and lower in frequency than the desired fundamental output. The sharp drop in alias magnitude is due to its frequency becoming 0 Hz.



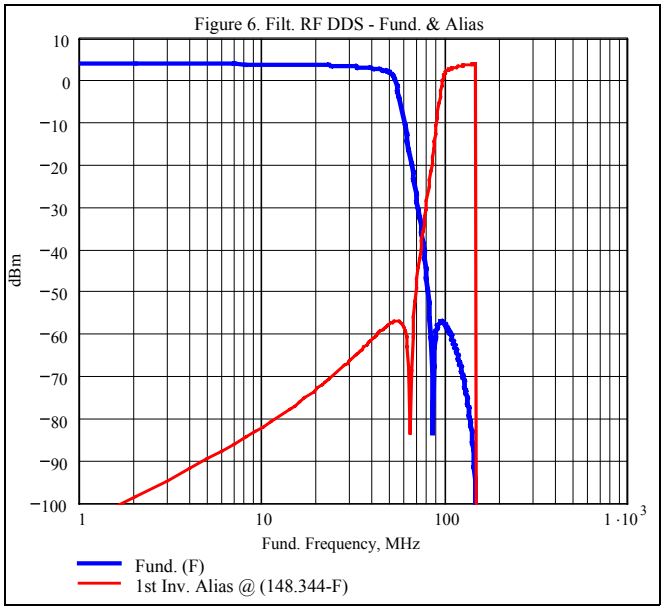

The primary function of an anti-alias filter is to reduce the amplitude of the 1st inverted alias to an acceptable level over the desired frequency range. Since both the RF and LO DDSs will have approximately the same relative amplitude for the 1st inverted alias, the VNA detector is vulnerable to a spurious DC mixer product if they are both not filtered.

There is an LC anti-alias filter to the RF DDS output at J170 and another to the LO DDS output at J180. The designs here are based on a seven-element Chebyshev filter with one added zero, as conceived by Jim Tonne, WB6BLD [9]. The modeled insertion losses for the RF & LO anti-alias filters are shown in Figure 5. The LO DDS filter was designed for slightly less attenuation above 50 MHz to maintain drive to the Detector LO input.




In both filters, the attenuation notch was positioned to roughly maximize the dB difference between the 1st inverted aliases and their corresponding fundamentals below 60 MHz.

Lastly, Figure 6 shows the modeled output amplitude of the fundamental and the 1st inverted alias. For fundamental frequencies below 50 MHz, the 1st inverted alias is at least –59 dBc. At 60 MHz, the 1st inverted alias is –48.5 dBc. Note that the fundamental modeled amplitude here agrees quite well with the measured data shown in Part 1.




The RF DDS filter attenuation notch is provided by C172 shunting L171. Additional capacitors, shunting the other two inductors, were investigated; but they were found to have undesired effects on return loss and fundamental amplitude. The single shunting capacitor offers an acceptable combination of fundamental and 1st inverted alias attenuations and return loss.

Note that there are other inverted aliases beyond the 1st that occur at (Fclk – N*F). For sufficiently high F, these higher order aliases come within the anti-alias filter passband, and are not rejected.

The decision not to on-board buffer the (difficult to replace) DDS modules was based on a desire to maximize return loss and minimize harmonics at the RF and LO primary PCB outputs. Any buffers, that were investigated, would adversely affect both characteristics significantly above those of the DDSs.

It was felt that user care & caution and the option of using external buffers would provide sufficient protection against accidental damage, in most cases. Posting the following or similar warning, somewhere in the work area or on the VNA, is also advisable:

**Connecting this VNA to an amateur transceiver or any other similar device capable of potentially damaging RF output levels, exceeding approximately +10 dBm, should be preceded by either disabling that device from generating damaging levels entirely or, at least, isolating it sufficiently via attenuation to ensure that the VNA is not exposed to damaging RF levels.**

This type of limitation is not uncommon. For example, the HP 8554B spectrum analyzer simply has "Maximum 10 dBm" adjacent to its RF input connector.

In addition to the limitation noted above for externally applied RF levels, there are also limitations on external applied DC voltages to the VNA. The RF DDS and the Detector RF & LO inputs are all transformer coupled, so each of these inputs is limited to externally applied 0 V DC. While the LO DDS outputs are both AC coupled via 1 uF, 25V, capacitors, a good rule of thumb would be to simply use 0 V DC for all connectors.

Any builder, wishing to extend the DC limitation to 25 V DC on all I/Os, could stand up 1 uF, 25V, SM capacitors on the PCB pads for the Detector RF and LO inputs and the RF DDS anti-alias filter output & wire J211, J210, and J170 respectively to the tops of the capacitors. This has not been tested, but calculations suggest that it should have only minor effects on VNA performance, mostly near 50 kHz.

The output impedance of all DDS outputs is nominally 50 Ω. See the Performance Summary in Part 1 for return loss plots for the DDS outputs at J170 and J180.

Master Oscillator Test Point

J150 provides an optional test point for the master oscillator. A resistor divider, comprised of R150, R151, & R153, provide an attenuated input to the AD8041, 160 MHz bandwidth, unity gain buffer [10]. The output series resistor, R152, provides source match as well as some short circuit protection for the AD8041.

The net effect of these components is to provide a –12 dBm level into 50 Ω at 148.3 MHz.

This test-point can also be implemented without the AD8041 buffer. Simply, eliminate U150, R151, R152, and R153. Add a jumper between the U150 lands pin 2 to pin 3 and another jumper in place of R152. Definitely use C151 to avoid DC loading of the internal oscillator up level. The result is also a –12 dBm level into 50 Ω at 148.3 MHz.

+5V Power Interface

J100 requires +5 V from an external power supply for the source side of the VNA PCB. Due to its relatively high current requirement, two pins are used for each of power and ground. C100-C103, FB100, and FB101 [11] provide input high frequency filtering as well as isolation between the analog and digital power section of the DDS modules.

Figure 2 contains:

- The VNA Detector.
- Detector Power Regulators

VNA Detector

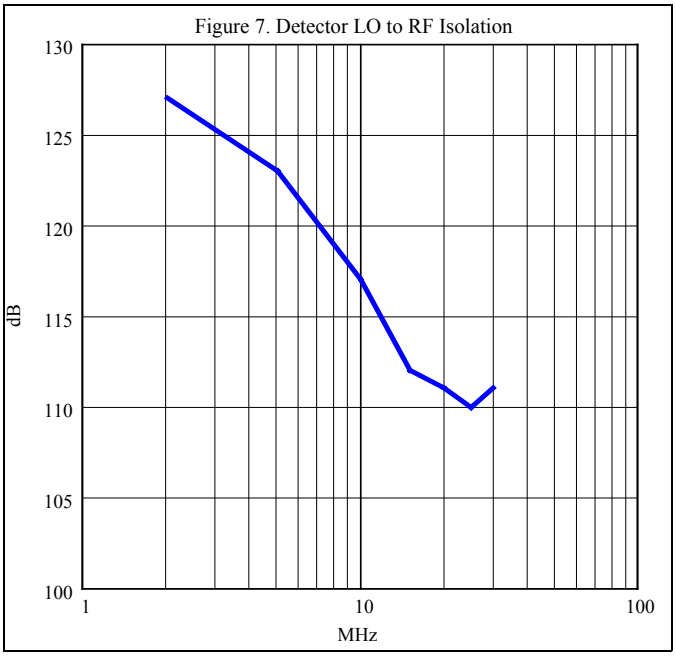
The VNA Detector function is implemented using a linearized Gilbert cell mixer, analog filtering & buffering, an analog to digital converter (ADC), and a precise and temperature stable +2.5 V voltage reference for the ADC.

The MC1496 [12] at U210 contains the basic Gilbert cell mixer. The Detector RF and LO Inputs to U210 are differentially coupled using 1:1 turns ratio transformers, T211 and T210. This improves LO-RF port isolation. Figure 7 shows the measured LO-RF isolation for the VNA Detector, which is about 60-70 dB better than the commonly used SBL-1 diode doubly balanced mixer (DBM).

There are sites for C210 and C211. These are no longer populated with capacitors and must be replaced with shorts.

C216 & C217, when combined with the leakage inductance of T211 as well as the reduced value of R213 to 47.5-Ω, provide improved Detector RF In return loss.

Figure 7. Detector LO to RF Isolation




The linearization of the Detector is provided by R216. There is only about 0.02 dB compression with the +4 dBm input from the RF DDS.

There is an analog filter in the MC1496 collector outputs comprised of R240, C214, R230, C215, R231, C230, R241, and C240. Together, these provide a differential output with a 3 dB bandwidth of 96 Hz and 40 dB/decade roll-off.

For +4 dBm at the Detector RF input and –2 dBm on the LO input, each at 1 MHz, the differential output is about +/-1.04 V DC for 0 and 180 degree phase differences between RF and LO inputs. At 90 degrees, the differential voltage is approximately zero. Equations (1) - (3) and the related text in Part 1 provide additional detail that shows how a complex measure of the RF input signal is determined.

As noted in Part 1, this filter bandwidth can not be made arbitrarily small as the delay needed to decay from a 1V DC output to 1 uV DC output (1 ppm) would significantly increase the overall measurement time. This delay is 20 RC time constants for this filter. With the current component values, the delay is about 20 ms and about 15% of the ADC conversion time. There is a parameter in the 'configuration' file that allows the user to control this.

The filtered, differential, output from the MC1496 is provided to a pair of low noise, low offset drift, rail-to-rail, unity gain buffers at U230 and U240 which are each an LT1677 [13]. Each buffer input swings approximately +/-0.52 V DC around +3.1 V DC for +4 dBm RF input and those levels are well within the buffer input range. R232 and R242 at the buffer outputs provide isolation from the ADC capacitive inputs.

The ADC at U260 is an LTC2410 [14]. It is a delta-sigma type converter with differential inputs lines for the converter and reference inputs. It has 140 dB rejection of the DC common mode for both the converter input and the reference. It also has an input line to control the frequency of a power line notch filter. The converter provides 24 bits in about 134 ms (60 Hz notch – 160 ms for the 50 Hz notch) via a 3-wire SPI type digital interface back to the PC via U160 and Q190.

The ADC voltage reference is U250, which is the LT1460-2.5 [15]. Absolute accuracy of this reference voltage is not significant since the ADC readings are only used relative to one another, and not with respect to an absolute voltage standard. However, the stability of its DC voltage with temperature is significant and this is suitably low at 10 ppm/°C. For a 1°C change in temperature, say between the calibration with the thru line and the measurement of a filter for insertion loss, that means the reference level would change by only about 0.0001 dB.

With this reference, the ADC will function with a maximum input range of –1.25 to +1.25 V DC. That range allows up to approximately +5.5 dBm at the Detector RF Input of arbitrary phase.

50/60 Hz ADC Notch Frequency

The LTC2410 ADC can place a notch filter at either 50 or 60 Hz. Since builders may have environments that are predominately at one or the other frequency due to local AC power, I ran a test to see how well the differential use of the ADC combined with its common mode rejection might provide sufficient rejection from available 60 Hz field sources while the ADC was temporarily enabled for the 50 Hz notch. The ADC sample rate changed from 6.8/sec to 5.7/sec confirming 50 Hz operation.

Then a variety of available 60 Hz magnetics, ranging from small power supplies to a tape recorder head demagnetizer, were brought in close proximity to the VNA PCB. The AC sources were turned on and off while monitoring the ADC output at both high and low levels. While the PC monitor reacted violently, there was no indication of any effect on the ADC readings.

These results combined with the ADC higher conversion speed with the 60 Hz notch suggest that the ADC be enabled with the 60 Hz notch, regardless of where it is used. However, if a user does find a dependency on measured VNA data in a 50 Hz power line area, then cutting the land to ground on pin 14 of the LTC2410 ADC, U260, and connecting pin 14 to +5V via a 1K resistor will move the notch to 50 Hz.

Detector Accuracy – Phase Linearity

By utilizing the 11.25° phase increment programmability of the AD9851 DDS sources, a test was performed at 10 MHz to determine the phase accuracy of this detector. In this test, the LO DDS is connected to the Detector LO Input and the RF DDS is connected thru a step attenuator to the Detector RF Input. A special PC program was written to collect & analyze the measured data.

First, an attenuator setting is selected. Then, the RF DDS is set to each of its 32 possible phase values, ranging from 0 to 348.75 degrees. At each RF DDS phase, the LO DDS phase is set to 0 and 90 degrees and the vector data collected is modified to account for detector offset, similar to the transmission measurement using the *Modified Response Calibration* described in Part 1. Basically, this is done by first measuring the detector offset with no signal applied to the Detector RF Input. Then subtract that value from each subsequently measured value to obtain a corrected value.

After all 32 corrected data points at this attenuator setting are obtained, a linear regression line was generated which provides the "best linear fit" of measured vs. programmed RF DDS phase. Then, all measured phases are compared against the regression line to find the maximum +/- deviations and those values are recorded.

The attenuator setting is then changed, and the entire process is repeated. The attenuator settings in this test ranged from 0 to 110 dB with the following nominal values: 0. 4, 7, 10,15, 20, 30, …, 110.

The results of this test are contained in the "Performance Summary" of Part 1 under Detector "m)". Those results show that this detector has a maximum deviation of 0.01 degrees from the linear regression line over a range of essentially noise-free input levels, from about –10 to –30 dBm. Below –30 dBm, the system noise floor takes an increasing toll on accuracy. Above –10 dBm, detector compression is estimated to cause the steadily increasing phase error to 0.07 degrees at +4 dBm.

Detector Accuracy - Magnitude

The *mean* of the 32 measured & corrected signal amplitudes for each attenuator setting in the above phase linearity test is also calculated at each attenuator setting and compared against the attenuation measured at DC using a power supply, precision source and load resistors, and a DVM. The *maximum* deviation is also recorded at each attenuator setting

The results of this test are summarized in the "Performance Summary" of Part 1 under Detector "l)". These test results are normalized to the thru line, which was the attenuator at 0 dB.

The 1st plot in "l)" shows the *mean* deviation from DC attenuation at each attenuator setting as plotted against Detector RF Input level in dBm.. While there appears to be an offset in the mean over most of the amplitude range, it is largely the result of the 0.016 dB compression in the detector at +4 dBm. If an alternate reference level, such as –20 dBm, is used, then the offset largely disappears. What this indicates is that for the most demanding VNA measurements, avoiding the 0 to +4 dBm range could potentially reduce the error by about 0.02 dB. However, with many DUTs there will be other sources of measurement error that will dominate. An example of this is shown in the "Transmission Accuracy" section of Part 1 where the expected error for a 20 dB return loss attenuator at low attenuations would be about 0.07 dB.

In addition, the second plot in the "Performance Summary" of Part 1 under Detector "l)" shows the effects of the system noise floor by using the *maximum* deviation from the measured DC attenuation. This behaves in a fashion similar to the corresponding phase plot.

While these magnitude and phase errors are attributed here solely to the detector, in actual fact these errors are the result of multiple hardware characteristics such as source and load match as well as attenuator return loss and possibly some non-linear effects in the RF DDS. However, the VNA test frequency and the attenuator were selected to lessen the effects of these other characteristics while still testing at a representative frequency. In the DC test, the resistance of the source and load resistors were 4-wire measured at 50.085 and 49.967 ohms respectively. These would be equivalent to source and load return losses of 61 dB and 69.6 dB. The RF DDS return loss plot in the "Performance Summary" of Part 1 suggests that a test frequency of 1.8 MHz would likely further reduce the effect of source match on these results, but perhaps would be a less representative frequency.

Detector Power Regulators

J220 provides a nominal +12V DC from an external power supply. The series regulator at U220 is an LP2951 [16]. It

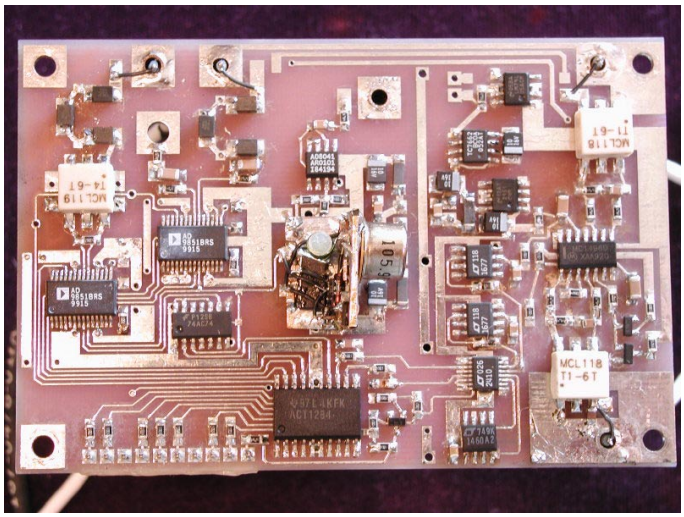
provides +5V DC to the detector. The nominal +12V DC is also supplied to U290 which is a TC7662B [17]. This is a DC-DC voltage converter that generates a negative DC voltage output that is slightly lower in magnitude than its positive input. The output of 290 in turn feeds U280, which is an LM79L05 [18]. U280 provides –5 V DC to the Detector, primarily the MC1496.

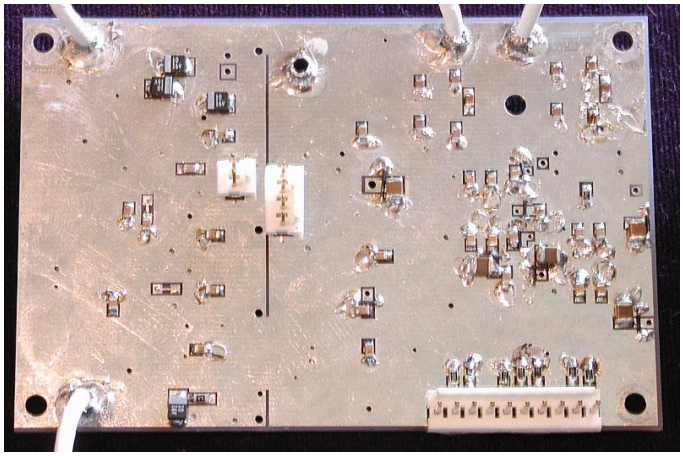
PCB Layout Considerations

Surface mount devices were used exclusively. For discrete components, 0805 size was the smallest used to facilitate build as much as possible while not adversely affecting performance.

Here are two photos of the VNA PCB with an early version of the homebrew master oscillator:

:





Since both source and detector functions are located on the same PCB, great care was taken during its layout to ensure ground plane integrity and isolation between these functions. Short wire jumpers that connect ground to ground across small island breaks in the ground plane around the DDSs are even called for to further augment ground plane integrity.

PCB Parts List

The Adobe Acrobat Reader used to view this document has a “Text Copy” facility. Potential builders should familiarize themselves with this facility as it can be used to copy part numbers from the parts list here directly to web pages for parts ordering in a largely error-free fashion.

Alternatively, there is a Lotus 123 spreadsheet file in the PCB ‘Build Info’ ZIP file that can be used in 123 or imported into other spreadsheet programs. Unlike the parts list here, the spreadsheet can be sorted in any desired fashion. Sorting by vendor or manufacturer’s part number, for example, would facilitate parts ordering as quantities needed of each part number are then readily seen. It may be desirable to perform these sorts on a copy of the file and preserve the original for other uses.

In addition to the web links provided in the Notes and the parts list, Digi-key frequently also shows manufacturer website info that may be of interest.

The SIP connector headers and receptacles shown in the parts list are gold and polarized to prevent accidental rotation, which could cause catastrophic hardware damage. These features are recommended.

**Homebrew Master Oscillator**

The schematic for the homebrew master oscillator L-shaped VNA circuit board is on Figure 8. Its parts list is also on Figure 8, and a ‘build info’ ZIP file is available at the website [19]. This ‘build info’ file also contains some useful master oscillator modifications and related build information, as provided by Ian White, G3SEK.

Circuit Overview

The homebrew master oscillator is a BJT-FET Butler oscillator, essentially patterned after one done by John Stephensen [20] based on its apparent ease of starting, low phase noise, and stability.

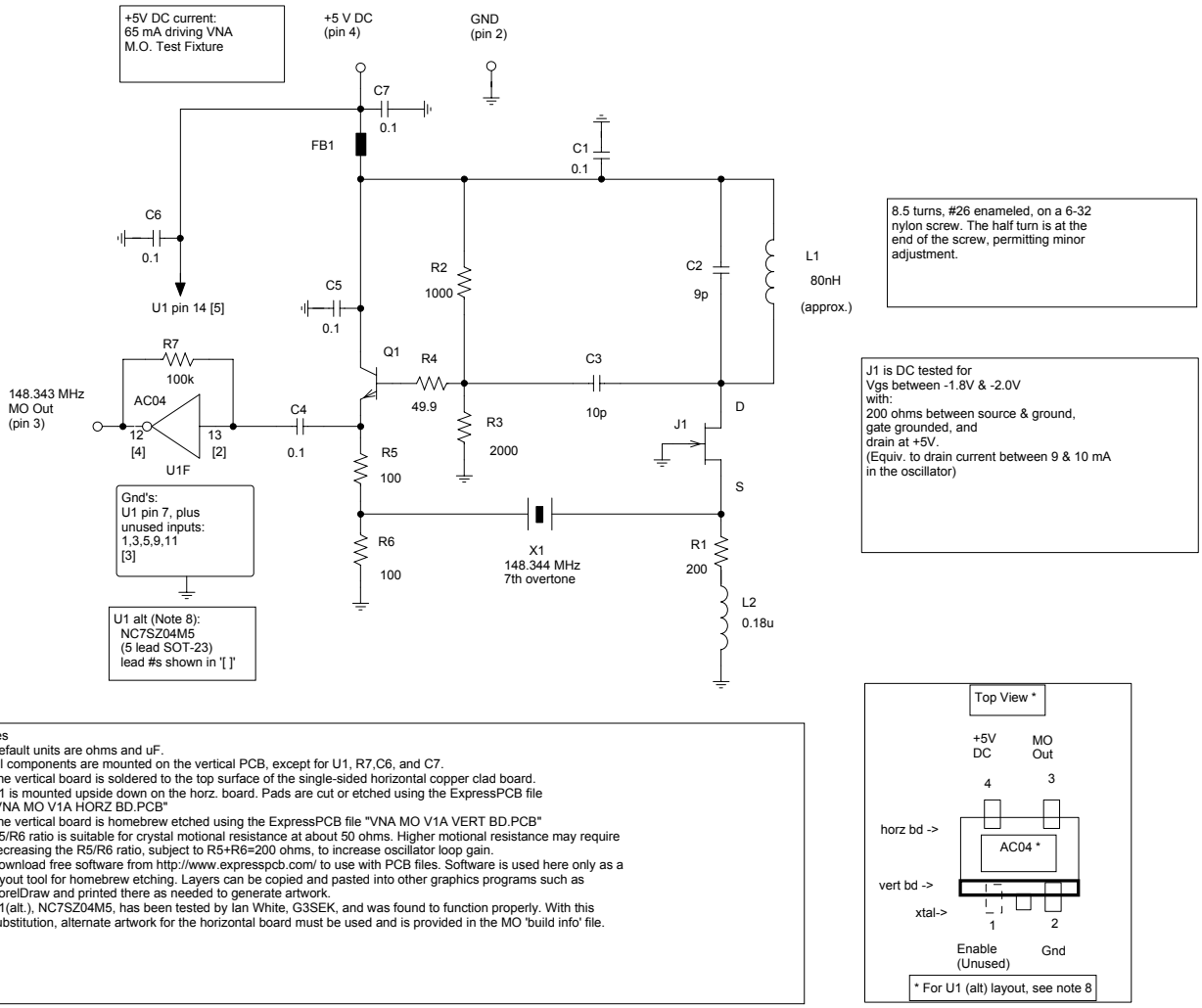
In this stripped down version, the varactor tuning function was eliminated to conserve space and that function is provided in software in any case. Also the tapped inductor was judged to be more difficult at this higher frequency and was replaced with other means of loop gain and tank Q control. As noted on Figure 8, the circuit functions reliably with crystal Rs of 40 to 50 ohms and the R5/R6 ratio can be used to increase loop gain to accommodate higher Rs crystals.

Again, to conserve space, the schottky diode clamp and associated components are eliminated and replaced by a FET DC sort, as noted in Figure 8, that controls the maximum drain current.

Lastly, in the interest of conserving space, also note that there is no explicit variable component to fine-tune the tank comprised primarily of L1 and C2. Instead, a half-turn on L1 overhangs the end of the nylon screw and its position is adjusted to ensure reliable starting and operation near the crystal series resonant frequency.

To adjust the half turn, the crystal is temporarily replaced by 50 ohms (or the actual Rs of the crystal) in series with 1000 pF, both surface mount and just long enough overall to make connection at the crystal pins. The oscillator is placed on the Master Oscillator Test Board described below and the L1 half turn is adjusted to obtain an operating frequency within about 0.5 MHz of the crystal frequency. If it will not oscillate at all near the crystal frequency, then the loop gain for the Rs used is most likely insufficient. In that case, R6 can be increased and R5 is decreased while keeping the sum of two at 200 ohms to allow the oscillator to start. Then the series RC is replaced by the crystal, and the half turn is further adjusted, if need be, to get the frequency within about 3 kHz (20 ppm) of the crystal series resonant frequency, most likely on the low side. It is important to have the actual operating frequency within about 3 kHz below the crystal series resonance to ensure oscillator stability with temperature and power supply variations.

# Figure 8. Homebrew VNA 148.344 MHz Master Oscillator (U140 on VNA PCB)




Notes
1. Default units are ohms and uF.
2. All components are mounted on the vertical PCB, except for U1, R7,C6, and C7.
3. The vertical board is soldered to the top surface of the single-sided horizontal copper clad board.
4. U1 is mounted upside down on the horz. board. Pads are cut or etched using the ExpressPCB file "VNA MO V1A HORZ BD.PCB"
5. The vertical board is homebrew etched using the ExpressPCB file "VNA MO V1A VERT BD.PCB"
6. R5/R6 ratio is suitable for crystal motional resistance at about 50 ohms. Higher motional resistance may require decreasing the R5/R6 ratio, subject to R5+R6=200 ohms, to increase oscillator loop gain.
7. Download free software from http://www.expresspcb.com/ to use with PCB files. Software is used here only as a layout tool for homebrew etching. Layers can be copied and pasted into other graphics programs such as CorelDraw and printed there as needed to generate artwork.
8. U1(alt.), NC7SZ04M5, has been tested by Ian White, G3SEK, and was found to function properly. With this substitution, alternate artwork for the horizontal board must be used and is provided in the MO 'build info' file.




Parts List:

| Designation | Description | Package | Manufacturer | Mfg P/N | Vendor | Vendor P/N |
|---|---|---|---|---|---|---|
| C1,C4,C5,C6,C7 | Ø.1 uF/5ØV/X7R/1Ø% | Ø8Ø5 | Panasonic | ECJ-2YBH1Ø4K | Digi-Key | PCC184ØCT-ND |
| C2 | 9 pF/5ØV/NPO/Ø.5p | Ø8Ø5 | Panasonic | ECJ-2VC1H9ØØD | Digi-Key | PCCØ9ØCNCT-ND |
| C3 | 1Ø pF/5ØV/NPO/Ø.5p | Ø8Ø5 | Panasonic | ECJ-2VC1H1ØØD | Digi-Key | PCC1ØØCNCT-ND |
| FB | Ferrite Bead | 18Ø6 | Panasonic | EXC-ML45A91ØH | Digi-Key | P11956CT-ND |
| J1 | JFET | SOT-23 | ON Semi | MMBFU31ØLT1 | Arrow | MMBFU31ØLT1 |
| L1 | approx. 8Ø nH | | homebrew | | | |
| L2 | Ø.18 uH/Shield/1Ø% | * | API Delevan | S121Ø-181K | Digi-Key | DN1Ø53CT-ND |
| Q1 | NPN transistor | SOT-143 | ON Semi | MRF9411LT1 | Mouser | 551-NE68Ø39R ** |
| R1 | 2ØØ/Ø.1w/1% | Ø8Ø5 | Panasonic | ERJ-6ENF2ØØØV | Digi-Key | P2ØØCCT-ND |
| R2 | 1.ØØK/Ø.1w/1% | Ø8Ø5 | Panasonic | ERJ-6ENF1ØØ1V | Digi-Key | P1.ØØKCCT-ND |
| R3 | 2.ØØK/Ø.1w/1% | Ø8Ø5 | Panasonic | ERJ-6ENF2ØØ1V | Digi-Key | P2.ØØKCCT-ND |
| R4 | 49.9/Ø.1w/1% | Ø8Ø5 | Panasonic | ERJ-6ENF49R9V | Digi-Key | P49.9CCT-ND |
| R5,R6 | 1ØØ/Ø.1w/1% | Ø8Ø5 | Panasonic | ERJ-6ENF1ØØØV | Digi-Key | P1ØØCCT-ND |
| R7 | 1ØØk/Ø.1w/1% | Ø8Ø5 | Panasonic | ERJ-6ENF1ØØ3V | Digi-Key | P1ØØKCCT-ND |
| U1 | Hex Inverter | SO-14 | Fairchild | 74ACØ4SC | Digi-Key | 74ACØ4SC-ND |
| U1(alt) | Single Inverter | SOT-23 | Fairchild | NC7SZØ4M5 | Digi-Key | NC7SZØ4M5CT-ND |
| X1 | 148.344 MHz crystal | HC-35/U | ICM | *** | ICM | *** |

* See the mfg drawing at http://www.delevan.com/PDF_DOCS/S121Ø.pdf
** This is an equivalent P/N. See Mouser at: http://www.mouser.com/
ICM - International Crystal Manufacturing, http://www.icmfg.com/, specify the P/N with the the 148.344 MHz frequency. It is low phase noise, 7th overtone, and Rs=1ØØ ohms max.
*** The ICM P/N for X1 is "35UAHHH32SAL-148.344"

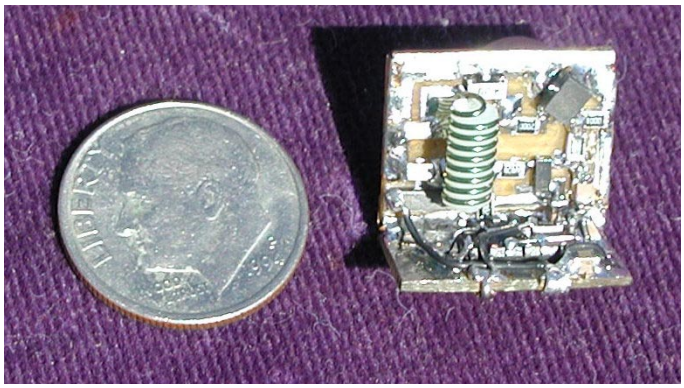
As noted above, precision tuning of the VNA master oscillator frequency is not required as that function will be provided in software.

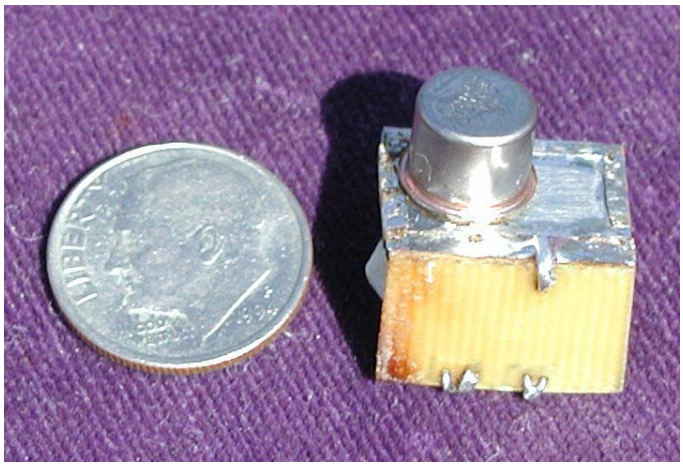
If a 1.3 GHz spectrum analyzer is available, here are some representative harmonic amplitudes at the MO testpoint, relative to the 'carrier' at the 148.344 MHz fundamental to compare new builds against:

| N | dBc |
|---|---|
| 2 | -25 |
| 3 | -18 |
| 4 | -35 |
| 5 | -25 |
| 6 | -34 |
| 7 | -27 |
| 8 | -29 |

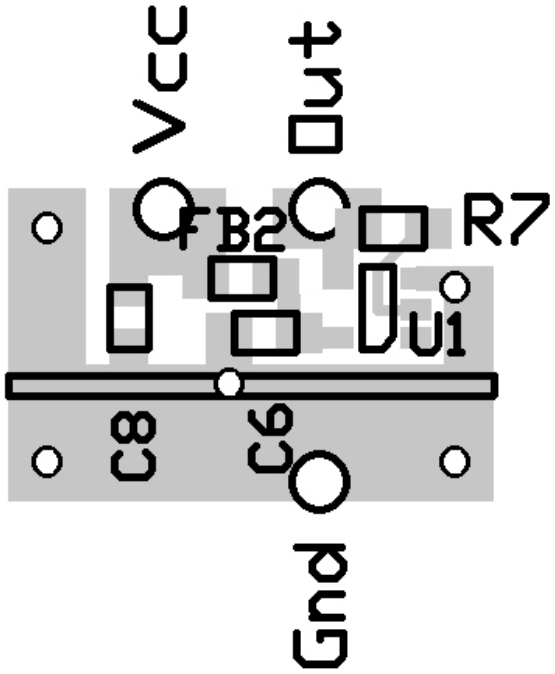
This unit also had a measured 47.5% duty cycle using the DVM ratio technique.

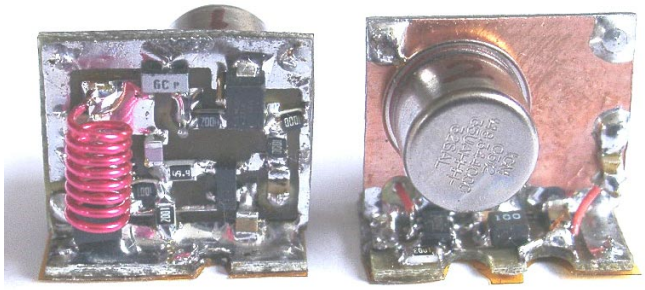
Here are two photos of the homebrew master oscillator:





While the side board is etched, the bottom board was constructed on single-sided copper clad board with the 74AC04 dead-bug wired. This was done to avoid a ground plane on the underside from shorting to VNA PCB conductors. To make the bottom board easier to construct, there has been some discussion about replacing the 74AC04 with a Fairchild TinyLogic part, such as the NC7SZ04M5, etching a double sided board, and using Kapton tape to prevent shorts. Here is a version built & tested by Ian White, G3SEK, that uses the TinyLogic part on a modified & etched bottom board:



See the Master Oscillator 'build info' file for additional details regarding Ian's modifications and build notes.

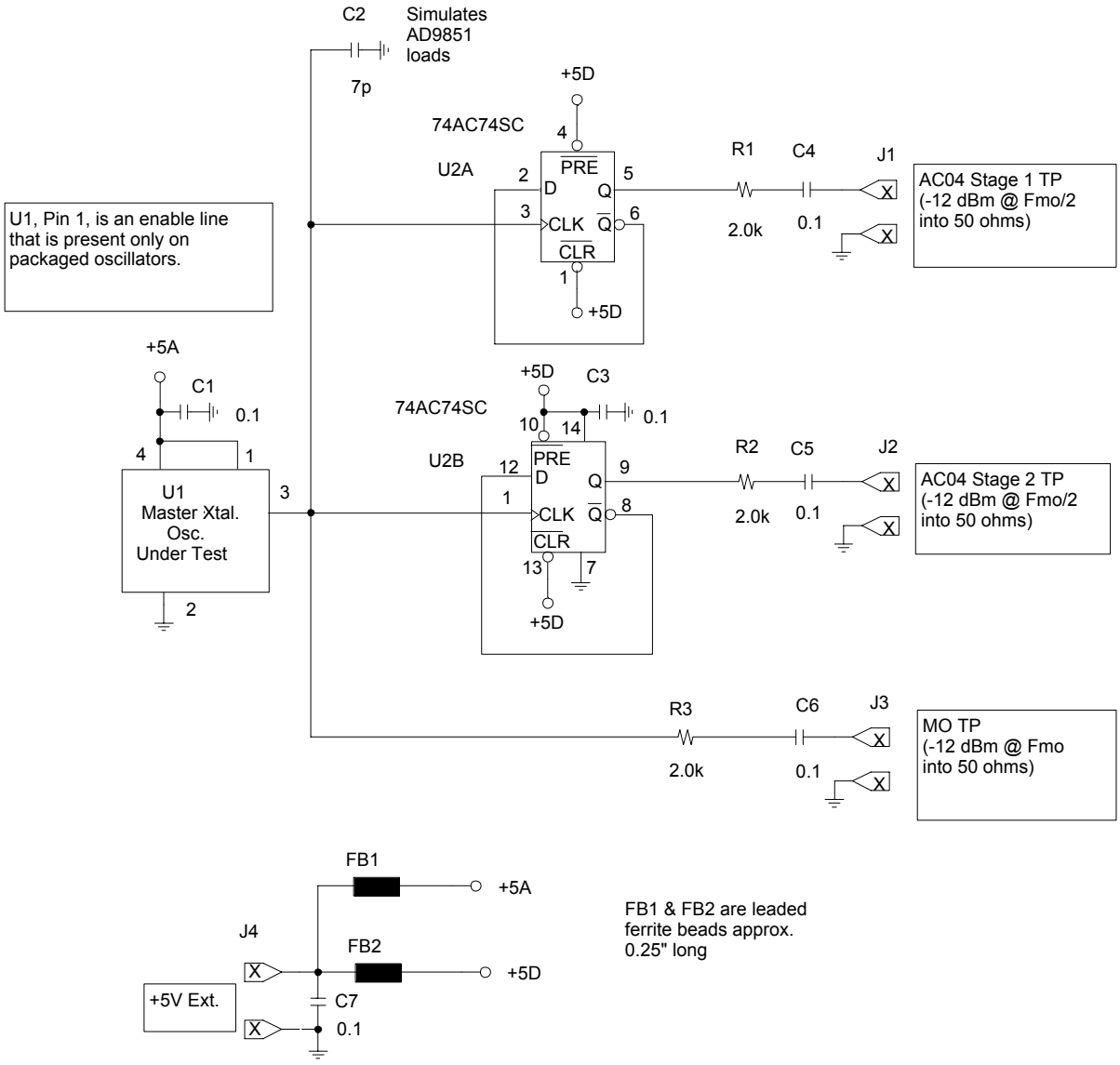
While two units were successfully built as shown in Figure 8 and the photos plus Ian's version, this circuit is highly vulnerable to stray capacitance and component tolerances. As such, it may require some experimentation to replicate with other parts.

**Master Oscillator Test Board**

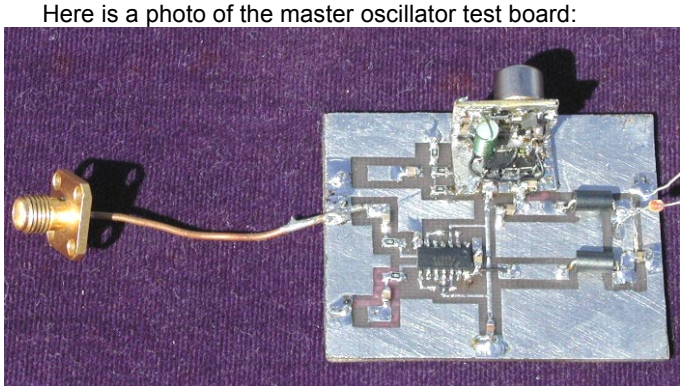
The Master Oscillator Test Board was designed to provide an environment to evaluate & test master oscillators without jeopardizing the lands on the VNA PCB.

The schematic for the master oscillator test board is on Figure 9. Its parts list is not shown, but this circuit uses parts shown on other lists. A 'build info' ZIP file is available at the website [21].

Figure 9. VNA Master Oscillator Test Board



Here is a photo of the master oscillator test board:



Circuit Overview

This test board was designed to simulate the loading the oscillator will see on the VNA PCB while simultaneously providing test points to observe its operation. It consists of the oscillator under test, a pair of D-type flip-flops each configured as a divide by two, and a capacitor that simulates the DDS loading. There are three test-points (J1-J3): one for each divider output and the master oscillator. These are attenuated and AC coupled outputs intended for termination in 50 Ω in a scope or a counter.

The 50 Ω far-end termination is mandatory; else reflections are likely to result in distorted waveforms and erratic counter readings. If desired, near-end terminations can be provided with 49.9 Ω 0805 resistors shunting J1 thru J3 and will further clean up the testpoint waveforms and a negligible effect on loading of the internal nodes. However, this will be at the expense of 6 dB less signal available.

With only the far-end termination, each output is about 120 mV pk-pk.

In addition, the internal oscillator output node and its 5V power supply pin can be probed with a short leaded 10 k-Ω resistor to a high impedance DVM. By measuring the average (DC) voltage at the output and power pins, the oscillator duty cycle can be approximated by their ratio [22].

Unlike the VNA PCB, each of the 74AC74 flip-flops are configured here as a divide by two to provide functionality readily recognizable on a counter or a scope. If a scope is used, its bandwidth should be about 350 MHz or higher to adequately see the detail in the 3.4 ns up and down times at J3. Lacking a scope of this caliber, a 1.3 GHz spectrum analyzer can also be used.

However, for most purposes, an accurate 150 MHz capable frequency counter and a DMM are sufficient for most evaluations to establish operating frequency, divide by two functionality, oscillator symmetry (45-55%), and oscillator power supply current. The oscillator power supply current is measured by temporarily lifting FB1 and inserting a low-drop current meter in series. This current is typically about 65 mA for the homebrew master oscillator alone when driving the test board load. The current meter should not be used during the other measurements.

Whether soldering the master oscillator to this test board or the VNA PCB, it was easier to solder the output pin first followed by the other 2 or 3 pins.

**Power Interface Board**

The power interface functions can be implemented in a variety of ways depending on the builder's preferences and possible use of available power supplies. These differences can generally be accommodated as long as the VNA power requirements in Part 1 are met. Relaxation of some of the requirements should be done with some care. In particular, the tolerance of the +5 V power supply should not be widened. Generally, increased ripple & noise may simply result in degraded spurious responses, but no attempt has been made to quantify this.

In addition to the power requirements in Part 1, potential builders might also want to plan for the possible future real-time detector as described in the Enclosure section below.

In general, it is recommended that power dissipation internal to the enclosure be minimized as much as possible. See the Enclosure section below for additional thermal design considerations. The use of an internal AC power supply is not recommended due to likely heat generation in 50/60 Hz magnetics. Off-line switching power supplies, while more efficient, are likely high noise level generators and are also not recommended for use internal to the VNA enclosure. However, DC-DC switchers can be used effectively if care is taken in packaging and filtering.

The schematic for a sample power board is on Figure 10. No parts list or 'build info' file is provided for this function as it largely depends on individual user preferences. However, the protection features and the burn-in & test recommendations should be followed for alternative implementations.

**A burn-in test of any power board, as indicated on Figure 10, is highly recommended to prevent catastrophic damage to the VNA PCB.**

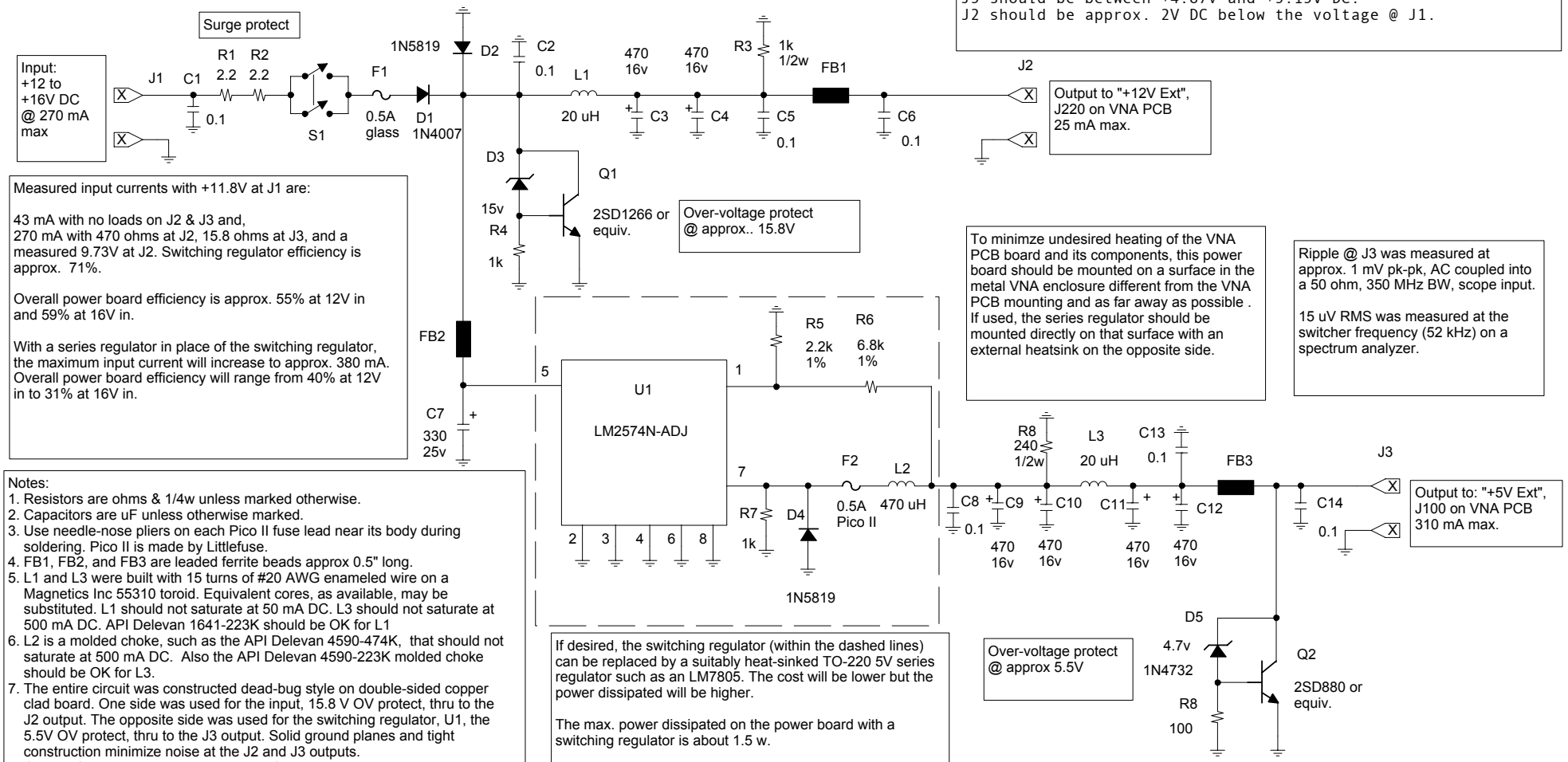
Circuit Overview

Referring to Figure 10, here are some circuit highlights. An external +12 V to +16 V DC power supply is supplied at J1. R1 and R2 provide surge current protection during charging of C3 and C4 while switch S1 is exercised with external power already applied. D1 and D2 provide reverse polarity voltage protection. L1, C3, C4, C5, FB1, and C6 provide primary ripple & noise filtering for the VNA PCB "+12V Ext." at J220. Over-voltage protection on this level is provided by D3, R4, and Q1. If approximately +15.8V at the cathode of D3 is exceeded, Q1 will draw current sufficient to blow fuse F1. C7 and FB2 also provide isolation of the VNA PCB "+12V Ext." from the +5 V switcher at U1.

The dashed lines surrounding U1, R5-R7, D4, F2, L2, as well as C8-C10, comprise the +5 V switching regulator. This regulator operates at approximately 50 kHz; newer parts operate at much higher frequencies. L3, C11-C13, FB3, and C14 provide additional filtering of ripple & noise for the VNA PCB "+5V Ext." at J100. Over-voltage protection on this level is provided by D5, R8, and Q2. If approximately +5.5V at the cathode of D5 is exceeded, Q2 will draw current sufficient to blow fuse F2. Some useful fuse info can be found on the web [23].

Construction of any switcher regulator over a solid ground plane, combined with suitable filtering on both input and output, is essential to obtain low output noise and the lower power dissipation than comparable linear regulators.

# Figure 10. Sample VNA Power Board (Switching Regulator Version)




```
Important!
----------
A 24 hour burn-in is recommended prior to connecting it to the
VNA PCB to minimize risk of PCB component damage. The burn-in
should be performed with 47Ø ohms/1w across J2, 16 ohms/3w
across J3, and a suitable DC power source @ J1 between +12V and
+16V DC. Periodic check of the DC voltages @ J2 and J3 and
component temperatures should also be done.

During this burn-in:
J3 should be between +4.87v and +5.13V DC.
J2 should be approx. 2V DC below the voltage @ J1.
```

Measured input currents with +11.8V at J1 are:

43 mA with no loads on J2 & J3 and,
270 mA with 470 ohms at J2, 15.8 ohms at J3, and a measured 9.73V at J2. Switching regulator efficiency is approx. 71%.

Overall power board efficiency is approx. 55% at 12V in and 59% at 16V in.

With a series regulator in place of the switching regulator, the maximum input current will increase to approx. 380 mA. Overall power board efficiency will range from 40% at 12V in to 31% at 16V in.

To minimze undesired heating of the VNA PCB board and its components, this power board should be mounted on a surface in the metal VNA enclosure different from the VNA PCB mounting and as far away as possible . If used, the series regulator should be mounted directly on that surface with an external heatsink on the opposite side.

Ripple @ J3 was measured at approx. 1 mV pk-pk, AC coupled into a 50 ohm, 350 MHz BW, scope input.

15 uV RMS was measured at the switcher frequency (52 kHz) on a spectrum analyzer.

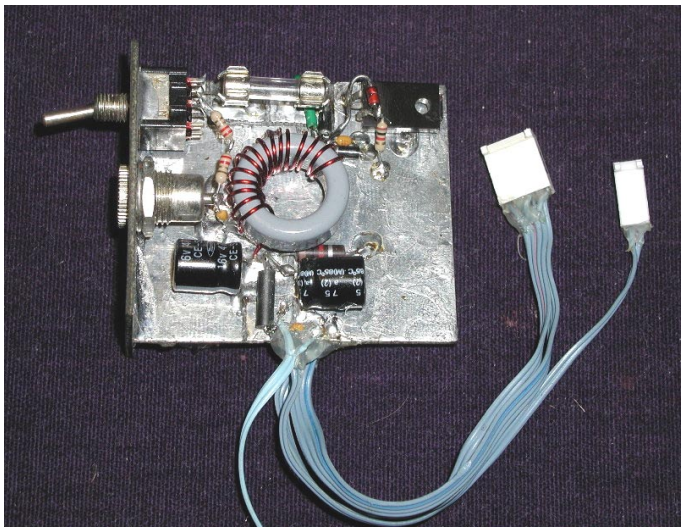
Notes:
1. Resistors are ohms & 1/4w unless marked otherwise.
2. Capacitors are uF unless otherwise marked.
3. Use needle-nose pliers on each Pico II fuse lead near its body during soldering. Pico II is made by Littlefuse.
4. FB1, FB2, and FB3 are leaded ferrite beads approx 0.5" long.
5. L1 and L3 were built with 15 turns of #20 AWG enameled wire on a Magnetics Inc 55310 toroid. Equivalent cores, as available, may be substituted. L1 should not saturate at 50 mA DC. L3 should not saturate at 500 mA DC. API Delevan 1641-223K should be OK for L1
6. L2 is a molded choke, such as the API Delevan 4590-474K, that should not saturate at 500 mA DC. Also the API Delevan 4590-223K molded choke should be OK for L3.
7. The entire circuit was constructed dead-bug style on double-sided copper clad board. One side was used for the input, 15.8 V OV protect, thru to the J2 output. The opposite side was used for the switching regulator, U1, the 5.5V OV protect, thru to the J3 output. Solid ground planes and tight construction minimize noise at the J2 and J3 outputs.
8. Q1 and Q2 can be virtually any NPN, TO-220, transistor with min. beta=100 and minimal heat-sinking.

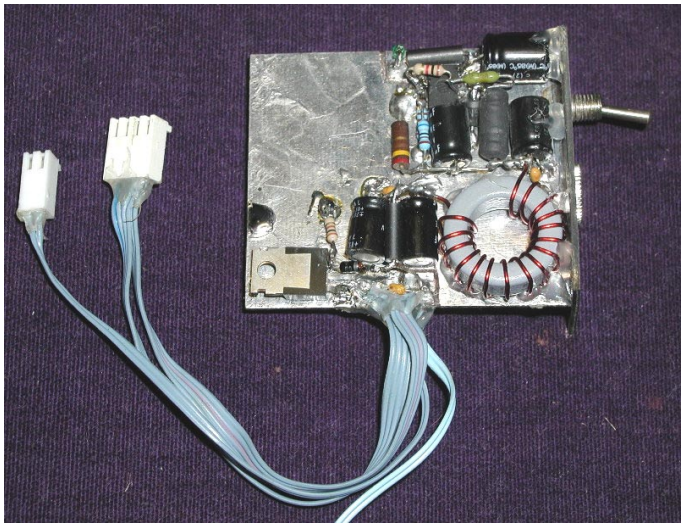
If desired, the switching regulator (within the dashed lines) can be replaced by a suitably heat-sinked TO-220 5V series regulator such as an LM7805. The cost will be lower but the power dissipated will be higher.

The max. power dissipated on the power board with a switching regulator is about 1.5 w.

With the series regulator, the power dissipation on the power board is about 3.0 w at 12V in and 4.2 w at 16V in

Here are two photos of the power interface board:





To minimize IR drops, the cables that are mated to J100 and J220 on the VNA PCB are soldered in place at the power board.

**VNA Signal & Power Connectors & Cabling**

RF Signal Interface

Possible connectors for the VNA RF signal interface are UHF, BNC, N, TNC, 3.5mm, 7mm, F, and SMA [24]. It was felt that SMA was the most desirable after weighing such things as size, electrical characteristics, repeatability, reproducibility, availability, compatibility with commercial VNA test sets and calibration standards, and cost.

Repeatability is a connector mating issue. The goal is that repeated mates of the same pair of connectors results in measured data that is consistently within some desired set of bounds - for example, bounds placed on |rho| and angle (rho). Repeatability is one reason why precious metals, such as gold, are used in commercial precision calibration standards. Repeatability also depends on the condition of the connectors, I.E. if their mating surfaces are worn out, dirty, oxidized, or corroded.

Reproducibility is a manufacturing issue that relates to connector geometry and materials used. In particular, the electrical length of the four connectors used for discrete component reflection measurements must match as closely as possible (three for OSL calibration standards and one for the discrete component). Excessive variation among these four, I.E. lacking some degree of reproducibility, increases the measurement error.

Electrical length depends primarily of the physical length of the connector and the dielectric constant of the insulating material in the connector. Matching of electrical length will be discussed further in the section on Calibration Standards.

SMA Use & Care

Regarding connectors and their care, there is much info on the web for the interested reader. Here are some key things to keep in mind for SMA connectors:

- Get the best your budget can handle. Ham flea markets are frequently sources of high quality SMA connectors and semi-rigid coax cable assemblies in reasonably good condition. There may also be similar sources on the web.
- Keep the connectors in good condition. Periodically inspect your connectors checking for overall cleanliness, oils, films, metallic flakes due to galling or abrasion of mating surfaces, etc. Cleaning with a new toothbrush, cotton swabs, alcohol, and compressed air, if available, is recommended.
- When initially bringing the mating connectors together, pay careful attention to alignment to avoid damaging the center pin or receptacle.
- Do not rotate the body of either connector, as that will cause abrasion of mating surfaces [25]. Note that the outer ferrule on the male SMA is not actually the mating shield contact and rotating it is preferred.
- Do not over-tighten connectors. The SMA torque spec is 5 inch-lbs. Torque wrenches are available for the well heeled [26]. Lacking a torque wrench, hang a known weight on a standard open-ended wrench such that it provides 5 inch-lbs while tightening the connectors. Then loosening it by hand might provide a crude calibration for the degree of hand tightening required.
- Rotating the connector bodies and over-tightening can result in significant connector damage.

SMA Connector Replacement

This is an issue that primarily affects bridge and enclosure connectors. Calibration standard and DUT connectors can be easily replaced when they are worn out. Bridge connectors are probably the next easiest as they can be generally unsoldered from the PCB. The enclosure connectors can be difficult if not planned for in advance. One option, that's been considered, is the use of flexible 50 Ω coaxes, each terminated in a male SMA at the front or back panel end & soldered into the PCB at the other end. These attach to female-to-female feedthru bulkheads, mounted on the enclosure panels from the inside. The outer interfaces of these bulkhead connectors take the majority of the wear. The bulkhead connector can be easily replaced, without any unsoldering & soldering, but access to both sides of the panel is required.

Another option, that may not require internal access, is the field replaceable SMA connector, as available from Johnson Components or Molex. As these parts are typically designed for microstrip, not coax, on the 'fixed' internal side. they will require an adapter designed to a) terminate the coax from the VNA PCB, b) provide the needed center pin to mate with the external SMA, c) provide impedance control, and d) provide shielding. To avoid the need for internal access during connector replacement, the mounting of this adapter on the inside of the panel will have to be independent of the screws used to secure the SMA connector on the outside. Mechanical complexity is reduced somewhat if the adapter and the SMA can secure each other, but this would likely require internal access during connector replacement.

The drawbacks of both of these approaches are added cost and perhaps poorer repeatability due to the additional interface. For now, I have opted for internal cables terminated in the external female SMA and will replace the cable assemblies as needed. Builders will have to define this strategy for themselves.

PC Signal & Power Interface

The connectors chosen for J100, J160, J220, and their mates have gold over nickel in the contact mating area. They were selected to maximize stability of DC resistance thru the contact. This is particularly important for J100, which along with its mate supply +5 V DC to the DDS sources from a regulator, external to the VNA PCB.

These connectors also offer polarity protection. While the pin assignments for J100 were made to prevent catastrophic damage due to an inadvertent 180° rotation, pin assignments for J160 and J220 do not offer similar protection. Polarity protection also helps in inadvertent offset plugs (one or more pins) as well.

If searching for connector substitutions, one should keep these considerations in mind.

A female DB-25 is recommended for the external parallel port interface on the enclosure. This enables the use of commonly available male DB-25 to male DB-25 terminated (IEEE 1284) cables for the VNA to PC interface. Internally, a suitable cable, such as a short ribbon, is used between the DB-25 and the mate to J160 on the VNA PCB.

**Enclosure**

In addition to the comments noted in the Power Board section above, it is recommended that all major heat sources internal to the enclosure have a low thermal resistance path to the enclosure exterior and then to ambient air via heatsinks as needed. A metal enclosure, with solid electrical bonding between all mating surfaces, is recommended for effective thermal design and RF shielding.

Attention paid to these aspects of the enclosure design will pay dividends in terms of reduced warm-up and subsequent drifting. The primary sensitivity to temperature is the detector offset voltage, which has been measured at –1.8 uV/°F after the initial warm-up. Solid shielding will also permit its use for ancillary applications, such as IP3 and receiver sensitivity measurements.

A future extension of this VNA to include a 2nd detector capable of higher speed frequency sweeps and measurements is being developed. Unlike the present detector which can provide real-time measurements only at one to seven frequencies, the aim of the 2nd detector is to provide the user with frequency sweeps fast enough to allow data at hundreds of frequencies to be displayed on the PC screen at sub-second refresh rates. This would provide a much-improved facility for real-time measurements and adjustments. The higher speed will result in less dynamic range, but that is typically an acceptable trade-off to obtain real-time adjustment of things like filter passband noses or return loss that may be only 30 to 40 dB.

While the outcome & timing of this extension is uncertain, a builder that is interested in this potential future capability might want to allow for it now while selecting the enclosure to house the current VNA hardware.

The present expectation is that the 2nd detector is likely to have the following features:

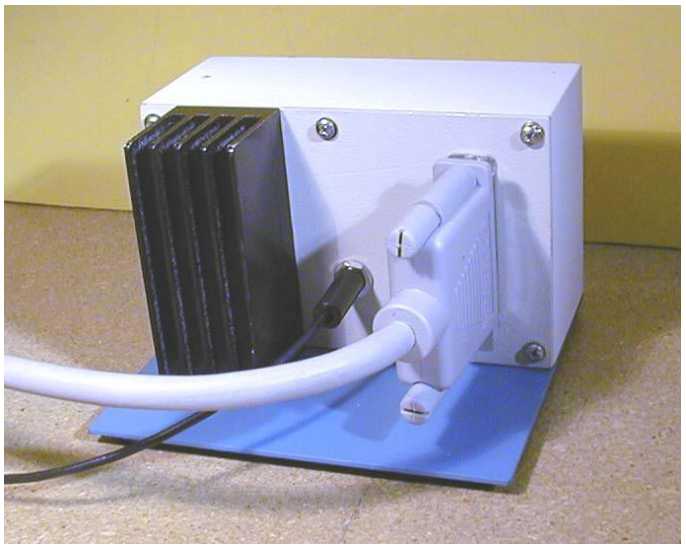
- Fits on the same size PCB as the current VNA ExpressPCB mini-board.
- Requires two additional SMA connectors on the enclosure front panel for its RF and LO inputs (see photo below).
- A 2 pin and a 10 pin connector as on the current VNA PCB for 12V power and its interface to the PC parallel port.
- Require less than 50 mA from +12V.
- Other enclosure back-panel connectors for functions like audio out to a PC sound card and a VCO control line for phase noise testing,
- Possible powering & control of analog mux switches or relays for an external test set that eliminates the need for DUT reversal for S11/S21 vs. S22/S12 and facilitates full 12 term error correction.
- Will require an external 2-way power splitter for the LO DDS when both detectors are required.

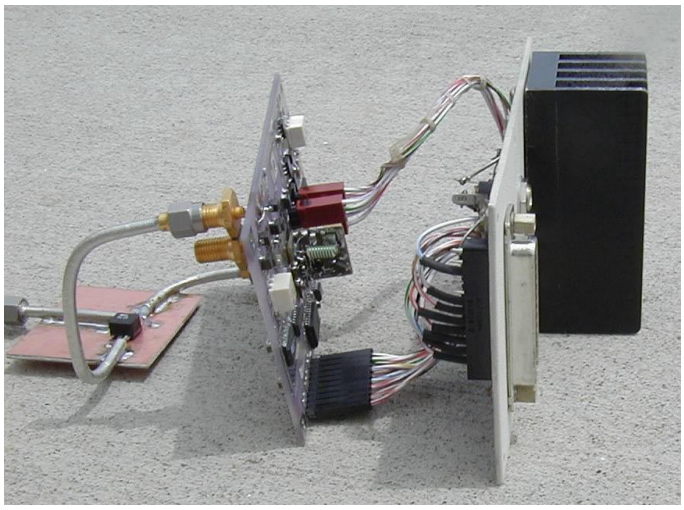
**In addition to the cautions noted above, it is advisable to locate a warning similar to:**

**Maximum:**
+10 dBm
0 V DC

**somewhere on the front panel of the VNA enclosure.**

For reference, here are some pictures of early VNA builds. Bill Carver, W7AAZ, built this one:



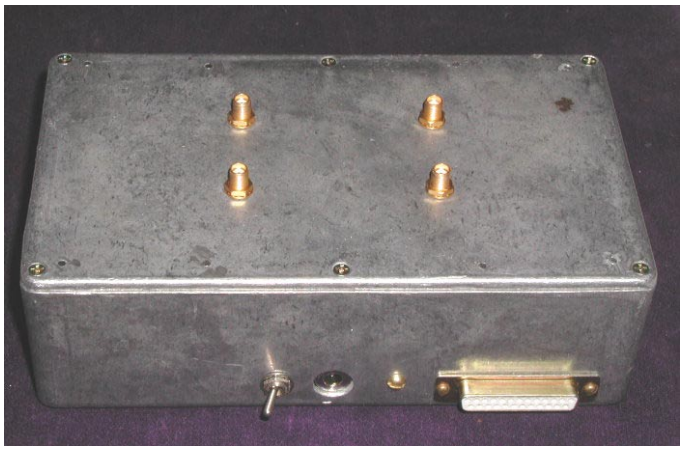
As can be seen in the above photo, Bill opted for an unusual mounting of the enclosure SMA connectors. Instead of using flexible cables between the enclosure front panel and the VNA PCB, he soldered semi-rigid coaxes directly in the holes on the VNA PCB. SMA connectors at the opposite ends of each semi-rigid coax provide the enclosure interface.

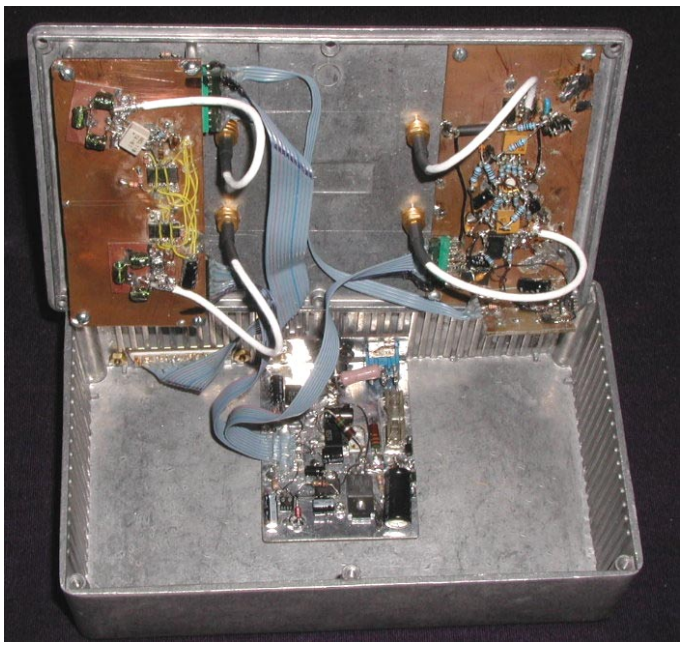
Here is another VNA, built by Harold Johnson, W4ZCB.



Harold included an internal AC power supply before the effect of internal heating on detector offset (-1.8 uV/°F) was understood. However, there is also an option to use an external +12 V power supply instead.

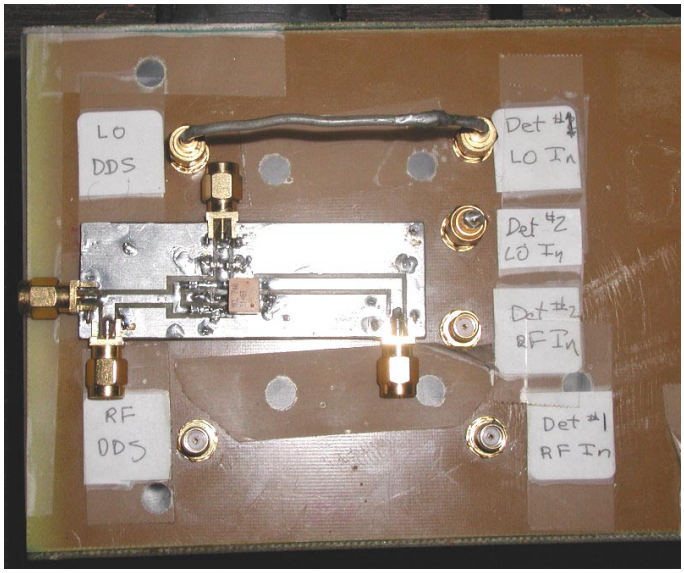
Here are a couple of photos of my prototype VNA which was done prior to the VNA PCB and was built dead-bug style. The 'fun' things to wire dead-bug style were the DDSs!





My PCB VNA is still in a development type enclosure to permit easy probing & modification of the circuitry - including

development of the 2nd detector. But here is its top panel, such as it is, along with a T1-6T reflection bridge laid on top:




While crudely constructed (and re-worked several times), my enclosure does illustrate two key points that a prospective builder, planning ahead for the 2nd detector, may want to incorporate:

- The spacing from the LO DDS Out (J180) to the Det #1 LO In (J210) and LO DDS Out (J180) to the Det #2 LO In are the same at 2.50 inches to allow one piece of semi-rigid coax to connect either pair without re-shaping it.
- Similarly, the spacing from the RF DDS Out (J170) to the Det #1 RF In (J211) and the RF DDS Out (J170) to the Det #2 RF In are the same, also at 2.50 inches, to allow one T1-6T bridge to connect either pair for reflection measurements or a 2nd semi-rigid coax could be used as the thru line calibration for transmission measurements using either detector.

The above connector designations are actually extensions of those on the current VNA PCB using flexible 50 Ω coax cables internal to the enclosure.

This connector arrangement would also allow for the 2-way LO power splitter when both detectors are required at the same time - for example, in 12-error term corrected two-port S-parameter measurements (assuming that the software for that is also developed!).

Note that the LO DDS Out connector at J180 shown above is the filtered one. While an optional on-PCB interconnect of the LO DDS Out to the Det. #1 LO In can be made, this interface is brought to the front panel instead for maximum flexibility.

The prototype VNA also has the 2.50 inch connector spacing to permit interchange of bridges and semi-rigid cables between the two.

My first configuration for the PCB VNA, as in Harold's & Bill's VNAs, used the on-PCB LO DDS to Detector path to minimize connector repeatability problems. Since then, additional applications and use conditions for the VNA hardware, including the expansion involving the 2nd detector, have been found that require making the LO path a front panel connection. The addition of SMA connectors in the LO path has not been found to cause accuracy or repeatability problems so far. It is likely that the LO path is less sensitive to connector repeatability than the RF path due to the saturation of the LO detector input.

The two circuit boards are vertically oriented with respect to the top panel; this was done primarily to facilitate probing from either side. Each side is exposed with the wiring & primary component side of each board facing outward. In addition, these board orientations also keep the center area of the enclosure and top panel open for the internal cables. The power board is mounted approximately centered right to left and on the bottom of the enclosure, in similar fashion to my prototype VNA. The back panel currently has the female DB-25, a coaxial slide-in type DC power connector similar to that on Harold's unit, and a power on/off switch.

In my finished version, I will likely opt to rotate my top panel to the front and use an enclosure that has a removable top lid, keeping the rest of the hardware in their current locations. The two printed circuit boards will remain vertical, one on each side, with the wiring & primary component side of each facing outward, still primarily to facilitate probing. The center of the front panel will have a connector layout similar to the current layout.

A suitable candidate for my finished enclosure is the Hammond 1458G5 [24], available from Digi-Key as HM346-ND. This should afford more than enough room. It's actually bigger than I would like, but I already have one available and, as Harold Johnson points out, too small an enclosure means it can get dragged about on the bench by the cables & DUTs attached to it. I will likely tie the front & back panels together with two internal panels that would provide for the mounting of each circuit board. Finger stock might also be required to obtain adequate shielding for certain uses – not generally VNA related.

In addition to the front panel SMA for the filtered LO output at J180, I would also provide a front panel SMA for the unfiltered LO output at J120. So that would be a total of seven female SMAs on the front panel – five from the current PCB and two more later for the 2nd detector. An SMA for the Master Oscillator testpoint output at J150 will likely be present on the back panel.

**Reflection 'Bridges'**

As indicated in Part 1, there are many possible candidates for the hardware that can be used for reflection 'bridges'. In fact, a well-balanced bridge when terminated with some load like 50 Ω is not even a requirement given the capabilities of Open-Short-Load (OSL) reflection calibration used in the software to be described in Part 3.

One bridge described here is a traditional bridge useful for general-purpose impedance measurements. Two other bridges are also described. One is optimized for low impedances and the other is optimized for high impedances, all relative to 50 Ω.

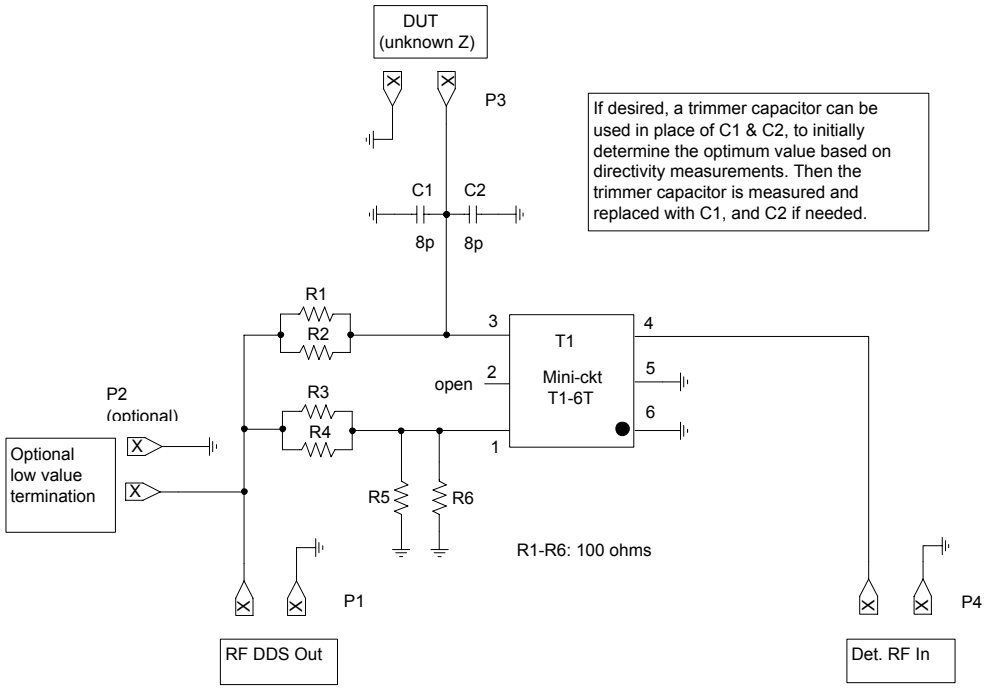
Due to the range of bridge options & potential use of different bridges optimized for various DUT impedances and need for DC biasing of active devices, it was felt that the bridge(s) were best packaged external to the main VNA enclosure. It has not been found to be generally useful to clutter the VNA front panel with additional connectors to support one or more internal bridges. Also, fewer connector interfaces and their attendant degradation in overall repeatability are required if the various bridges are connected directly to the VNA RF ports.

Part 3 will show some measured data using each of the three bridges described below.

T1-6T Bridge

Figure 11 shows the schematic and parts list for the T1-6T bridge, so named for its use of the Mini-Circuits transformer. A 'build info' file can also be found at the website [28]. However, the 'build info' will only be optimally usable, as is, if the prospective builder adopts the 2.50 inch spacing between the "RF DDS Out" SMA and the "Det. RF In" SMA connectors on the VNA. The bridge is equipped with male SMAs which permit it to be directly connected to the female connectors on the VNA. Of course, semi-rigid coax could be used in place P1 and

# Figure 11. T1-6T Reflection Bridge



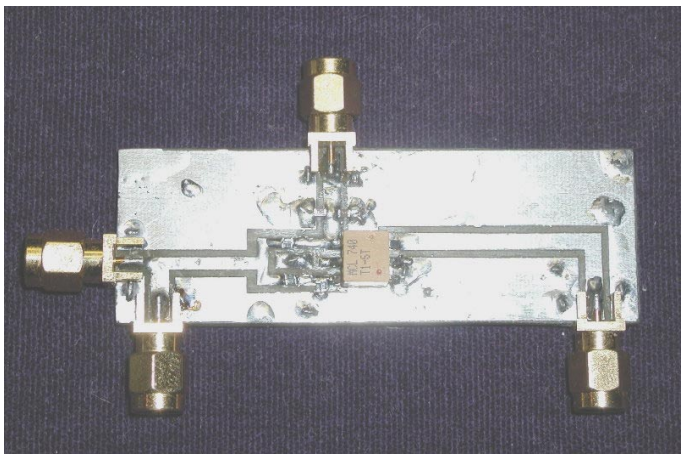

Notes:
1. P2 is optionally used to connect a low valued termination such as 4.7 ohms for a small improvement in measurement accuracy below about 0.5 MHz.
2. P1-P4 are edge mounted with 0.060" double sided copper clad PCB between the center pin and two ground pins.
3. See "T1-6T Bridge.PCB" for artwork. Plugs P1 & P4 are 2.50 inches apart and are intended to mate directly with identically spaced jacks on the VNA enclosure.
4. Bridge directivity is not critical if Open-Short-Load (OSL) calibration is used.

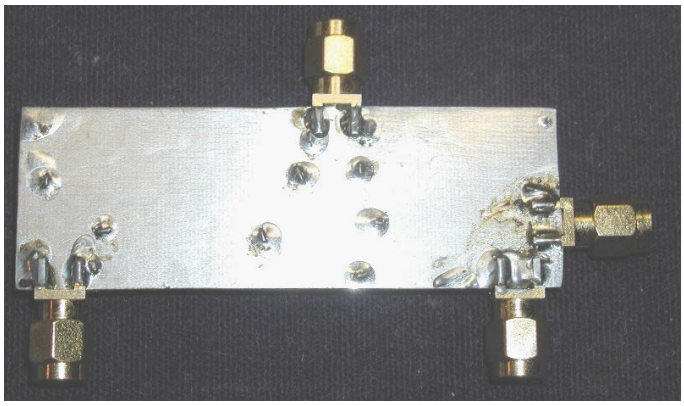
Parts List:

| Designation | Description | Package | Manufacturer | Mfg P/N | Vendor | Vendor P/N |
|---|---|---|---|---|---|---|
| C1,C2 | 8 pF/5ØV/NPO/Ø.5p | Ø8Ø5 | Panasonic | ECJ-2VC1HØ8ØD | Digi-Key | PCCØ8ØCNCT-ND |
| P1-P4 | SMA Plug | PCB | Amphenol | 9Ø1-9895-RFX | Mouser | 523-9Ø1-9895-RFX |
| R1-R6 | 1ØØ/Ø.Ø6w/Ø.1% | Ø6Ø3 | Panasonic | ERA-3YEB1Ø1V | Digi-Key | P1ØØYCT-ND |
| T1 | 1:1CT T.R. Xfmr | KK81 | Mini-Ckt | T1-6T-KK81 | Mini-Ckt | T1-6T-KK81 |

Amphenol - http://65.244.34.14Ø/Customer%2ØOutline/C9Ø1-9895-RFX.pdf
Digi-key - http://www.digikey.com/
Mini-Ckt - Mini-Circuits, http://www.minicircuits.com &
http://www.minicircuits.com/cgi-bin/spec?cat=tranfrmr&model=T1-6T&pix=x65_w38.gif&bv=4
Mouser - http://www.mouser.com/

P4 on the bridge to allow the bridge to conform to other VNA connector spacings. P1-P4 are all male SMAs. The DUT port at P3 can be calibrated with female SMA calibration standards, described below. Here are two photos of the T1-6T bridge:





One construction detail, common to all of the homebrew etched boards, can be noted above. Top and bottom ground planes are connected together with short wire jumpers thru the board and soldered on each side. This is an *essential* feature of good RF construction.

This bridge is a true bridge which is well-balanced with 50 Ω on its DUT port and approximately equal reflection coefficient magnitudes with an open and a short on its DUT port. It is useful for general-purpose impedance measurements. It is the recommended bridge if only one is to be built.

R1-R4 on Figure 11 are each 100 Ω, 0.1%, SM resistors. They were selected, along with C1 & C2, to maximize bridge directivity (I.E. balance) over the 0.05-60 MHz frequency range of the VNA. C1 & C2 were experimentally determined and can be left out initially. Bridge directivity is not essential to accuracy, given OSL calibration, but it is desirable to aid in visualizing and 'sanity checking' the measured calibration standard and DUT raw data as it is being collected. SMA P2 is an optional connector that can be used to add a fixed low value resistor across the RF DDS output. Its utility is a steady, but slight, improvement in measurement accuracy as the frequency is reduced from about 0.5 to 0.05 MHz. The resistor's primary beneficial effect is to reduce harmonic distortion. It also adversely affects source match. The result of that is that the measured reflection coefficient magnitude for an open on the DUT port is somewhat different from that of a short. Again, this is not critical to accuracy, but it does cloud user interpretation of measured raw data. If that frequency range is not of interest, then P2 is not needed. This bridge can be calibrated with the same open, short, and 50 Ω load standards used with the T1-6T bridge.

Low Z 'Bridge'

Figure 12 shows the schematic for the low-Z 'bridge.' It is only a bridge in a narrow sense, in that 'balance,' as measured by a null in the detector voltage, is nominally achieved only with a true short on the DUT port. With the DUT shunting the mainline from the RF DDS source to the detector, this bridge has maximum sensitivity for low impedances since these impedances exercises the dynamic range of the VNA detector, just as 50 Ω exercises the detector dynamic range on the T1-6T bridge. As in the T1-6T bridge, the low-Z 'bridge' is equipped with male SMA connectors. It can be calibrated using the same open, short, and 50 Ω load standards. User interpretation of raw measured data is a general recognition that lower detector voltage magnitude implies lower DUT impedance. There's potentially a small offset in that the series inductance represented by dimension "D" in Figure 12 can be series resonated with a higher (capacitive) DUT impedance than might be its actual minimum. This has no effect on the data collected and reduced as a result of the OSL calibration – only on user interpretation.

Artwork to homebrew a printed circuit board for this bridge has not been generated yet, but that can be readily done using the PCB file for the T1-6T bridge as a starting point.

High Z 'Bridge'

Figure 13 shows the schematic for the high-Z 'bridge.' It too is only a bridge in a narrow sense, in that 'balance' is nominally achieved only with a true open on the DUT port. With the DUT in series with the mainline from the RF DDS source to the detector, this bridge has maximum sensitivity for high impedances since these impedances exercises the dynamic range of the VNA detector. As in the previous bridges, the high-Z 'bridge' is equipped with male SMA connectors and can be calibrated using the same calibration standards.

Artwork to homebrew a printed circuit board for this bridge has not been generated yet, but that can be readily done using the PCB file for the T1-6T or the low-Z bridge as a base.

Currently, both the low-Z and high-Z bridges are implemented here using one surface wired board and some solder bridges to re-configure it.

**Calibration Standards**

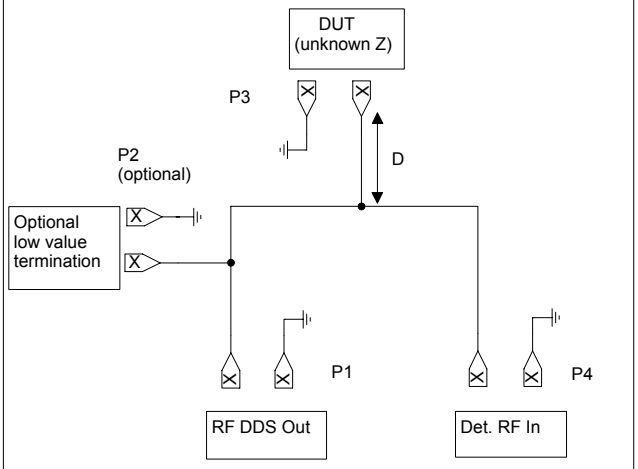
Once the source harmonics and detector non-linearities are made as low as possible, the key to VNA measurement accuracy lies in the type of calibration done, the quality of the calibration standards used, and the extent to which their impedances are 'known.'

Commercial VNA calibration standards can be very expensive. Fortunately, for the 0.05 - 60 MHz base range of this VNA, calibration standards can be built that are of surprisingly good accuracy, as was indicated in the Performance Section of Part 1. With care, they are also quite good thru 500 MHz.

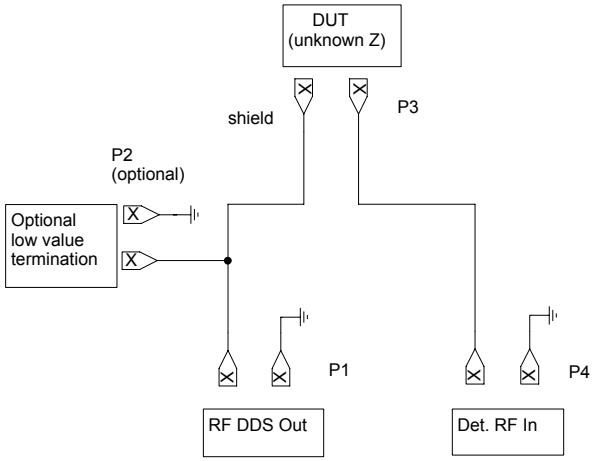
Part 3 will also show how certain parameters in the configuration file that relate to the calibration standards can be used by the software to account for known limitations in constructed standards.

An understanding of the discussion in Part 1 regarding reference and calibration planes for reflection and transmission measurements will be assumed for what follows, so refer back to that as needed.

## Figure 12. Low-Z Reflection Bridge




## Figure 13. High-Z Reflection Bridge




Common to both bridges:

Notes:
1. P2 is optionally used to connect a low valued termination such as 4.7 ohms for a small improvement in
   measurement accuracy below about Ø.5 MHz.
2. P1-P4 are edge mounted with Ø.Ø6Ø" double sided copper clad PCB between the center pin and two ground
   pins.
3. P1 & P4 are 2.5Ø inches apart and are intended to mate directly with identically spaced jacks on the
   VNA enclosure.
4. OSL calibration is required.
5. The high-Z bridge can be used only on 'floating' loads.
6. "D" should be as short as possible to maximize low impedance accuracy.

Parts List:

| Designation | Description | Package | Manufacturer | Mfg P/N | Vendor | Vendor P/N |
|---|---|---|---|---|---|---|
| P1-P4 | SMA Plug | PCB | Amphenol | 9Ø1-9895-RFX | Mouser | 523-9Ø1-9895-RFX |

Amphenol - http://65.244.34.14Ø/Customer%2ØOutline/C9Ø1-9895-RFX.pdf
Mouser - http://www.mouser.com/

OSL Reflection Standards

Since discrete component measurement is one of the primary interests with this VNA, the reference plane definition used here is the precise location of the open, short and load calibration impedances. As such, it does not include the connectors on which the discrete component and the calibration standards are mounted.

Later, the software configuration file may be expanded to allow the user to define offset delay, Zo, and loss parameters that, in effect, move the reference plane (the place with known impedances) to the calibration plane which is normally defined as the "seating plane" or the "outer conductor mating surface" between two connectors. As a result, data could be reported with respect to the connector seating plane and allow comparison with data collected from commercial VNAs or the current reference plane. Providing the software to accommodate these additional parameters is straightforward. Providing the numerical values required is not.

In any case, the construction of the calibration standards would remain the same. Regardless of whether measured reflection data is reported with respect to the current reference plane or seating plane, the reproducibility of these offset parameters among the four connectors used for a reflection test affects the overall quality of the calibration standards.

Commercial calibration kit data for 3.5 mm connectors (similar to SMA, but more precise) suggest that the short is the most precise, largely frequency independent, known impedance, standard. One kit definition lists its short standard low frequency stray inductance as 0.0021 nH [29]. So, it provides the best definition of the reference plane location. Any offsets among the relative locations of the calibration load impedances and the unknown impedance will cause calibration errors, which largely go undetected and increase measurement error. One offset can be detected however. The open calibration standard used as a DUT after calibration and temporarily shorted to determine how closely it matches the short calibration standard.

Here are two photos of the homebrew SMA calibration standards:

These are left to right:

1. Open
2. Short
3. 4x200-Ω, 0805
4. 4x200-Ω, 0603
5. 2x100-Ω, 0603
6. 4x200-Ω, 0805, white side up

All resistors are 0.1% and available from Digi-Key [30].

To start the construction of the calibration standards, we select a part with a captivated center pin, since commercially machined parts will provide a higher degree of reproducibility, I.E. consistency of electrical characteristics. In particular, the dielectric constant, physical length, and hence electrical length must be consistent among the four connectors used in a reflection measurement. This electrical length is essentially the offset delay referred to above. Also, machined parts will have a higher degree of diameter reproducibility & stability which, combined with dielectric constant, define the offset Zo. It is clearly desirable to have essentially one value for this for all four parts. Reproducibility of the offset loss depends on the quality of the conductors used. Connectors with a precious metal plating are recommended.

Since the bridge DUT port is assumed to be equipped with a male SMA connector, we will select female SMAs for the calibration and DUT connectors. Here, we use the Amphenol 901-144-8RFX [31], but there are several other suitable parts available. These are gold-plated brass, gold-plated beryllium-copper, and Teflon dielectric.

All three calibration standard connectors have their center pin, and the dielectric, if raised on a particular connector, carefully ground or milled down to be flush with the back surface of the shield conductor. The fourth connector, used for the DUT, is ground or milled down in similar fashion. If desired, it can have a 30-50 mil nub left on the center conductor to make it easier to solder a DUT to later. This nub should be eliminated for DUTs that don't require it, like surface mount devices.

**During the grinding or milling operation, the connector should be mated to a male SMA connector to keep all pieces in proper alignment.**

If present, the four corner shield posts can be ground down as well, but I chose to leave them on for some mechanical protection. I used a Dremel grinding wheel that just fit between the four corner posts.

The connector to be used as the open calibration standard remains as is after the grinding operation. It has fringing capacitance that will be accounted for in the software configuration file. The low frequency value for the 3.5 mm connector is 0.049 pF [29] and 0.039 pF was determined for my open calibration standard as tested by Chip Owens & documented in Part 1.

The connector to be used as the short calibration standard has a solid thin copper or tin foil circular plate that is just large enough when placed over the back end of the connector to be soldered to the center conductor and the entire ground conductor perimeter. All mating surfaces are pre-tinned with a thin coat of solder to allow re-flow soldering on essentially unexposed surfaces. This standard is assumed to have a stray series resistance and inductance that can be accounted for in the software configuration file.

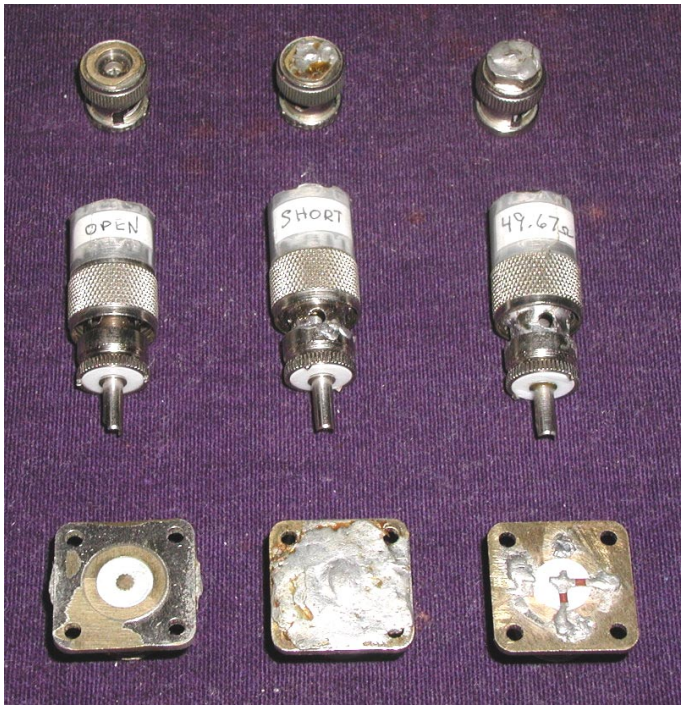
The connector used for the 50 Ω calibration standard has two 100 Ω, 0.1%, 0603 SM resistors soldered in diametrically opposed locations. 50 Ω load standards using four 0.1% 200 Ω 0805 or 0603 resistors, mounted in N-S-E-W fashion around the center conductor, have also been tested and yield fairly good return loss and correctable in any case using the software configuration file. I have had some difficulties with the 2x100 Ω 0603 standard in that the center pin eventually breaks loose with erratic contact. So, while it is the most accurate, it hasn't been as durable to date for me as the 4x200 Ω standards. The 50 Ω load standard is assumed to have a stray inductance in series with the load resistance value, shunted by a stray capacitance – all accountable in the software configuration file.

The models assumed for the calibration standard stray parameters should provide good accuracy thru 500 MHz, assuming accurate values are known.

Part 3 will discuss the software configuration file and its parameters. Values for various calibration standard stray and resistor parameters will be provided there.

These construction techniques can be applied to male SMAs [32] as well.

This technique of calibration standard construction is not limited to SMA connectors. Here is a photo of similar techniques being applied to homebrew standards on BNC, UHF, and N connectors that are useful for testing antennas and other hardware:




In the BNC open, a wire was soldered to the center pin that matches the length of the short; since the end of the wire is not secured, a bit of glue holds the center pin in place in the dielectric. In the BNC 50 Ω load standard, a 49.9 Ω 1% axial leaded 1/4w resistor is mounted coaxially with one end soldered to the visible shield end plate; the other end is soldered to the center pin.

The UHF barrel was cut just below the holes to permit an internal shorting plate to be soldered to match the location of the open center pin. The barrel was then carefully re-soldered while maintaining alignment to allow the outer ferrule to function properly. The UHF 50 Ω standard was constructed using four 200 Ω, 1%, ¼ w, axial leaded resistors that were inserted through each of the four holes and soldered to the center pin and hole perimeter.

Only half of the N connector 50 Ω standard is actually present with only two of the four 200 Ω resistors needed.. Since I now have a close approximation to a commercial standard, I use this as a 100 Ω standard.

Mating these to the bridge SMA DUT port will require adapters. Coax cable can also be inserted between the bridge DUT port and any set of calibration standards where the DUT will also be placed. The OSL calibration will correct for these additions, although possible changes in flexible coax should be considered for the most critical applications.

Only 50 Ω load standards have been considered so far. Other values can also be used as long as the software configuration file contains the appropriate value. The software configuration file also permits an independent change in the system Zo – I.E. the impedance that is used as the basis for reported reflection coefficients. While this can be done without changing the bridge itself, there are certain other connector issues that have to be carefully considered to get meaningful test results.

While OSL calibration corrects, in principle, for fixture, bridge, and VNA related linear errors, there are practical limitations to what can be done - even with ideal calibration standards. For example, one should not expect good measurement accuracy if a 40 dB 50 Ω attenuator is placed between the bridge DUT port and the actual point where the DUT and calibration standards are attached. In this case, all measured reflections would be very nearly the same. The error correction software would have its work cut out for it and actually would not do very well at all due to signal to noise ratio and ADC resolution. While this is clearly an extreme case, one should still not get sloppy or cavalier with fixture or bridge design or optimistic with their expectations regarding calibration. It is generally worth making any new set-up as good as possible and testing it with a known load impedance to get an idea of its accuracy.

Discrete Component Connectors

As noted above, to maximize impedance measurement accuracy, and related parameters like R, L, and C of discrete components, the reference plane of the component under test must match as close as possible to that of the OSL calibration standards, which are in turn matched to each other. So they are mounted on connectors that are identical to the calibration standards.

For critical component measurements, such as on surface mount components, where lead strays are critical in the end use application, the components under test should be soldered directly to the DUT SMA with the appropriate lead lengths.

For less critical measurements and/or to facilitate quick checks that can be supplemented later with more accurate fixturing if needed, one could solder small sockets or perhaps clips to the DUT SMA. These sockets or clips would accommodate some standard DUT lead diameters. While this would greatly decrease test time, the resulting would depends on whether the strays associated with the sockets or clips are significant to the test results at the test frequency(ies) of interest. Calibrate once and then test all of the DUTs.

Thru Transmission Standards

Currently the thru line is assumed to be zero delay and matched to the Zo specified in the software configuration file. As such there are no parameters defined for it specifically. This essentially corresponds to the reflection reference planes being in the same place for a two-port network. This is quite closely satisfied by a female-to-female SMA thru standard with the same overall length as two of the female reflection SMA connectors arranged back-to-back. If precisely matched, then that is the ideal that basically discounts the connectors for all four S-parameters. This can be particularly useful, for example, if coax cable without connectors is the desired DUT.

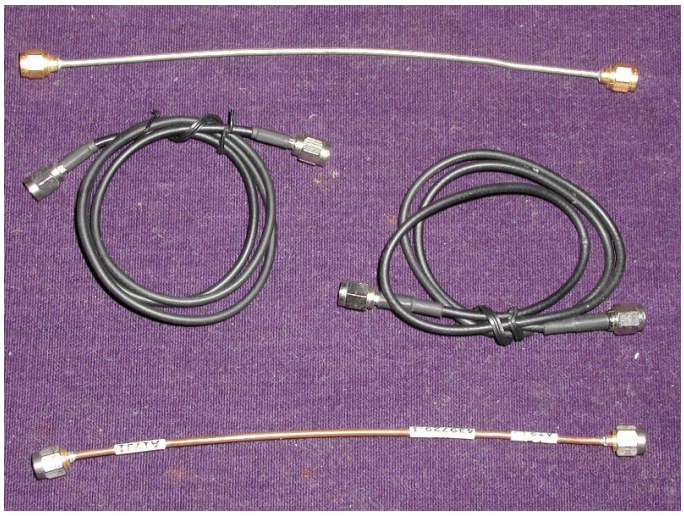
Even if this is not satisfied precisely, the net effect is a slight error in transmission phase angle. Whether that error is significant depends on how the S21 (and S12) data is used. For many measurements, such as gain measurement or even group delay below 60 MHz, error in the pico-seconds will likely be insignificant. However, if all four two-port S-parameters are

being used to convert to two-port Y, H, or Z parameters, then the phase angle error may become important.

Later expansions of the software configuration file will likely provide for parameters defined for this calibration standard as well. As in the reflection standard enhancements, the software is the easy part while providing the required numerical data may not be.

**Miscellaneous Cables**

Semi-rigid and flexible coax can be used to extend the VNA DUT port(s) to the actual DUT location:

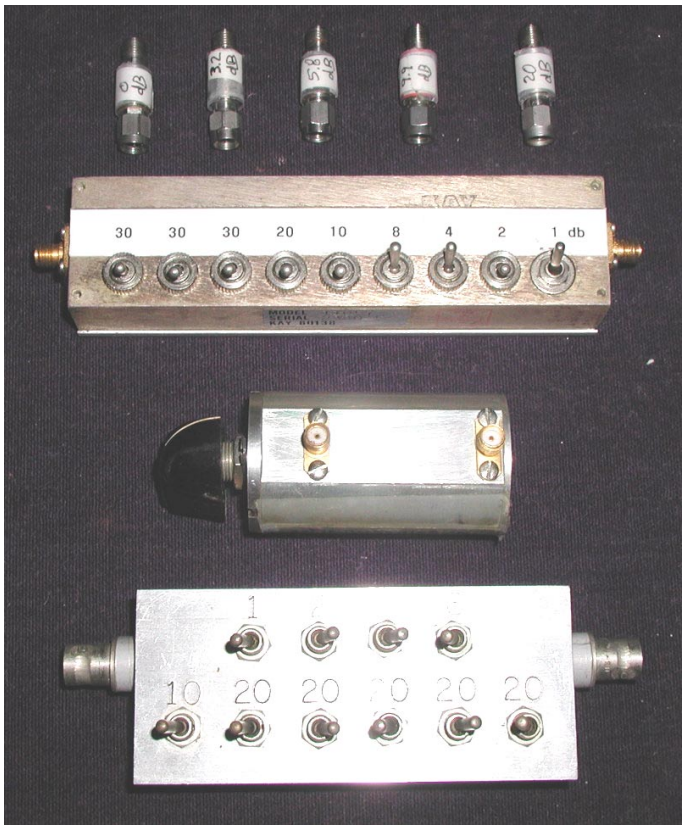


OSL calibration will correct for these additions. In critical applications, semi-rigid coax is preferred as its characteristics are less likely to change if the cables are moved between the calibration and DUT steps in a measurement. These changes would result in measurement error since they involve hardware that is being calibrated out of the picture.

There are surplus sources of 50 Ω 85 mil and 141 mil OD semi-rigid cables. I personally prefer the 85 mil coax.

**Fixed/Step attenuators**

A collection of attenuators is useful for certain DUTs that are subject to overload and also to reduce the output of certain DUTs so they don't overload the VNA:




With semi-rigid or rigid connector interfaces, 0 dB attenuators are handy to mechanical match other attenuators in a set-up.

**Coaxial Adapters**

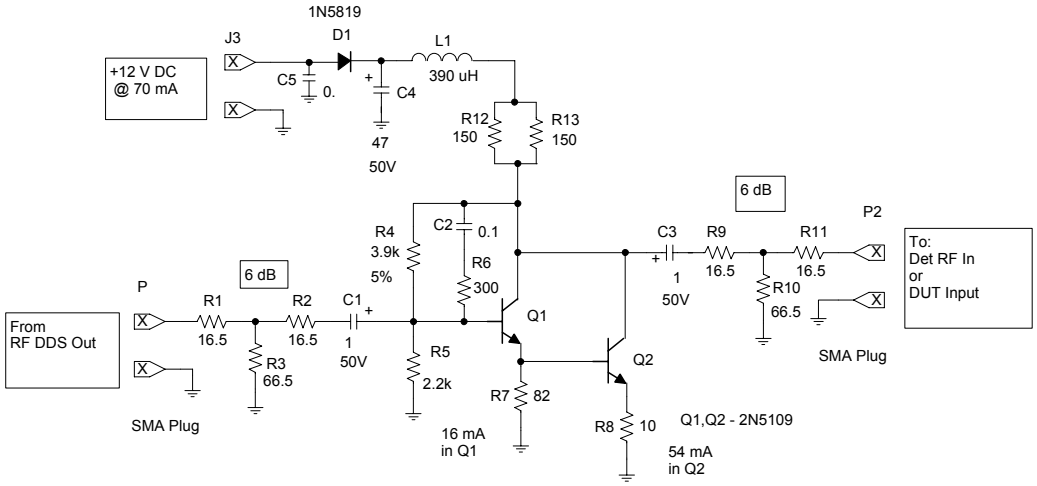
As noted above, a collection of coaxial adapters can be useful for testing in connector environments other than SMA:

While adapters can be cascaded, it is generally better for repeatability, stability, and accuracy to minimize the number in series. Calibration standards that correspond to the DUT connectors will reduce the effects of adapter Zo mis-match, but instability in multiple connector interfaces will cause unpredictable increases in error.

**RF DDS Buffer**

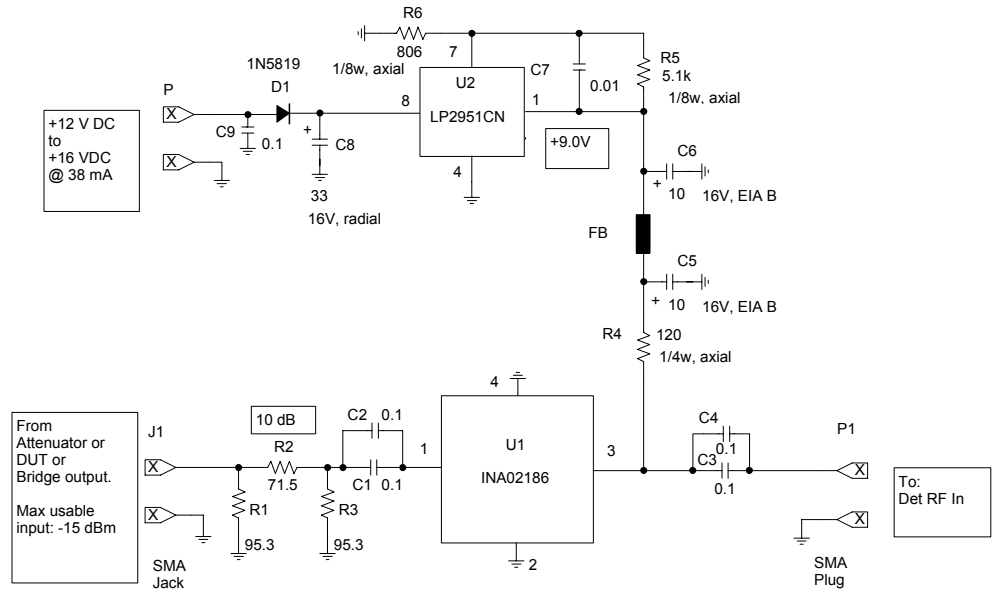
The RF DDS Buffer is shown of Figure 14. It is a nominal over-all 0 dB gain block with output return loss exceeding 35

## Figure 14. RF DDS Buffer: 2N5109 Version




Notes:
1. Resistors are ohms, 1/4w, and 1% unless marked otherwise.
2. Capacitors are uF unless marked otherwise.
3. L1 is a molded choke, such as the API Delevan 1641-394K, that should not saturate at 75 mA DC.
4. The entire circuit was constructed dead-bug style on double-sided copper clad board. Q1 & Q2 cans are insulated from the ground plane by a small piece of electrical tape.
5. This circuit is a discrete version of the Agilent MSA-1105 with the feedback capacitor increased to permit operation down to 50 kHz.
5. Performance (with input from RF DDS):
   Gain: Nominal 0 dB +0.3 dB/-0.5 dB over 0.05 - 60 MHz
   Output Return Loss: > 35 dB, 0.05 - 50 MHz; > 28 dB, 50 - 60 MHz.
   Harmonics: better than -48 dBc, 0.05 - 60 MHz, highest is the 2nd harmonic.

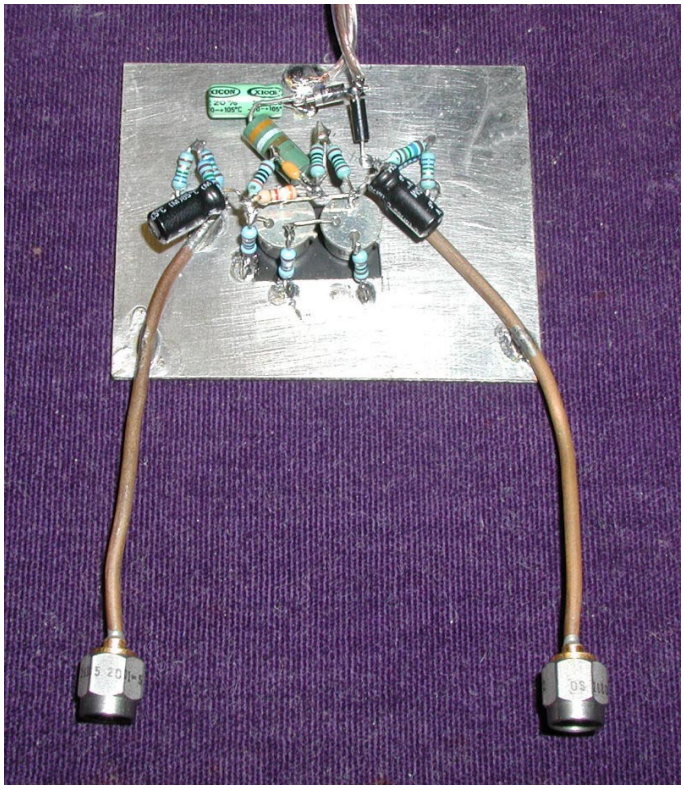
## Figure 15. Detector Pre-Amp: INA-02186 Version




Notes:
1. Resistors are ohms, 0805 SMD, and 1% unless marked otherwise.
2. Capacitors are uF & 0805 SMD unless marked otherwise.
3. The parallel capacitors at C1/C2 & C3/C4 can be replaced by single 0.22 or 0.33 uF if available.
4. The entire circuit is constructed as a combination of "dead bug" and etched patterns for the SMD components on double-sided copper clad board.
5. A segmented 50 ohm Zo microstrip line is used between J1 & P1. Keep the top surface metal on either side of this line for grounding using a grid of wire pass-thru's between top & bottom layers (see photo). The shells of J1 & P1 are also connected to the board planes on both sides. Some builders also solder copper foil around the board perimeter that connects top and bottom board ground planes.
6. Ground lead inductance on U1 must be kept very low to avoid instability - see the Agilent datasheet at:
   http://literature.agilent.com/litweb/pdf/5965-9675E.pdf
   Although Agilent recommends boards no thicker than 0.032" , no instability problems were seen with 0.062" board with a ground land pattern under U1 that connects the two top surface ground patterns together along with four pass-thru ground wires from the board top to bottom plane that surrounding U1 as close as possible.
7. Performance :
   Max Output: 2V pp square wave when input is over-driven
   Gain: Nominal 21 dB, flat to within +/-0.1 dB over 0.05 - 60 MHz
   Input Return Loss: > 34 dB, 0.05 - 0.15 MHz; > 40 dB, 0.15 - 45 MHz; >33 dB, 45 - 60 MHz with its output to the VNA Det. RF In.
   Harmonics (0.05 - 60 MHz fundamental):

| Input Lvl | 2nd Harm. | 3rd Harm. |
|---|---|---|
| -15 dBm | -31 dBc | -45 dBc |
| -20 | -36 | -55 |
| -25 | -41 | -65 |

dB, 0.05-50 MHz, and 28 dB, 50-60 MHz. Here is a photo of a temporary build:



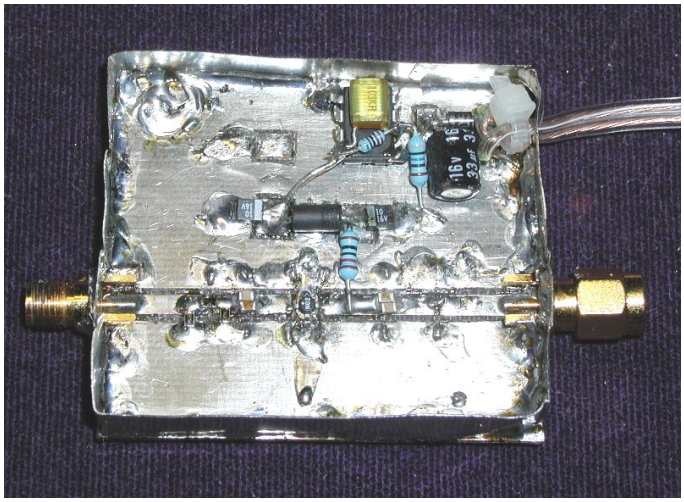
It can be placed between the RF DDS output and a DUT input. It serves two primary functions:

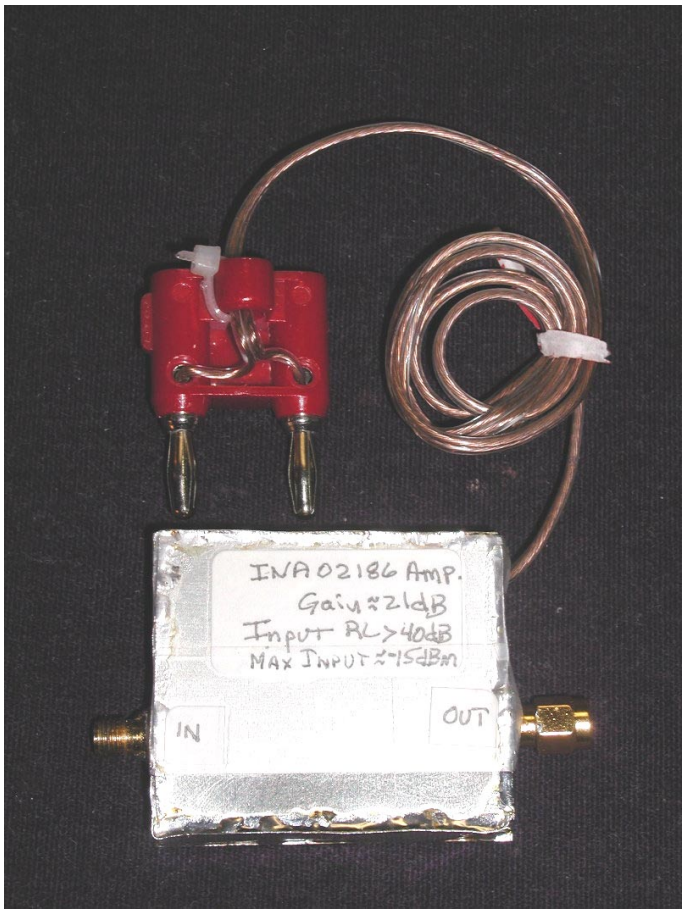
- Provides better source match than the RF DDS over the full frequency range and can improve measured S21 accuracy.
- Provides protection of the RF DDS in the event of accidental overload.

The downside is that its harmonic levels are higher at some frequencies. As such, it should not be used routinely unless its effects in a given measurement are clearly understood & acceptable.

**Detector RF Pre-amplifier**

The Detector RF Pre-amplifier is shown on Figure 15. Here are two photos:






It has a nominal overall 21 dB gain, >45 dB return loss for 0.15- 45 MHz, and can be used with up to -15 dBm at its input. It can be placed between a DUT or bridge output and the Detector RF input and serves three primary functions:

- Its gain helps improve the signal/noise of DUTs such as a filter in stopband or the reflection from an active component that requires a low-level signal to avoid non-linearity.
- Provides better load match than the Detector RF Input over the full frequency range and can improve measured S21 accuracy.
- Provides protection of the Detector RF Input in the event of accidental overload.

As the RF DDS buffer, it can also increase harmonic levels depending on input level and should be used with care.

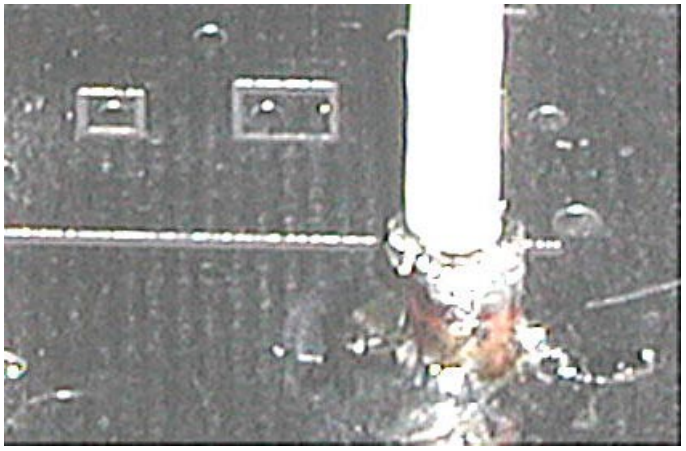
**Construction**

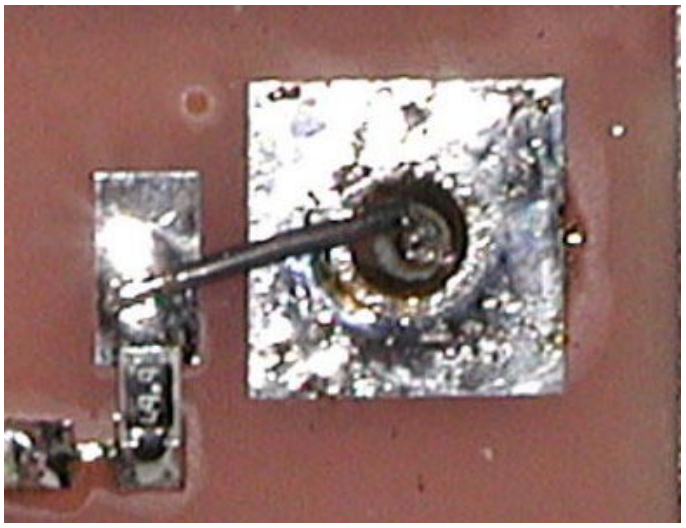
<u>VNA PCB Build Notes</u>

Following are some notes that may be helpful to the prospective builder. There are additional notes in the VNA PCB 'Build Info' PDF, which were provided by Ian White, G3SEK. Ian describes, in detail, the build sequence that he employed during his construction. These too may be helpful to the prospective builder.

1. The two schematic pages should be used as the primary document to resolve any apparent discrepancies. If that does not help, then contact the author.
2. Use the VNA PCB 'Build Info' PDF file. Print out its pages, in landscape for maximum size, and staple them together as indicated.
3. Have hardcopy of the schematics, parts list, drawings, and photos available during build. When I did my build & soldered a component down to the board, I yellow marked it on the schematic & the layout. That way it was easy to tell if I missed anything. One could also yellow mark it on the parts list.

4. Familiarize yourself with all available documentation. All three forms of viewing the PCB - schematics, drawings, & photos - can be used, as best suits each builder (but trust the schematics the most). I addition, the parts list is useful, not only for ordering, but build as well.
5. By aligning and stapling the first four layout drawings, one can create a sort of x-ray view of the board. Two bottom plane drawings are provided - one view from the front(top), the other from the back(bottom). There are another two pages for the bottom layer that can be stapled together with the print facing each other to aid in placing components on that side.
6. The smallest text size that ExpressPCB permits was used, but it was not small enough in all cases to precisely place the component designations where they belong. Use the schematics & photos to aid in correct component placement.
7. The populated PCB photos have proved also useful. The photos should be used as a general guide for confirmation and with some care. Completely current high quality photos are not available. As a result, some components may not be correct. Again, use the schematic to resolve all discrepancies.
8. On the virtual silkscreen drawing, the "[" prefix on the component ID tells you that component is on the "Bottom."
9. The location of the "+" for polarized caps (CXXX+ or +CXXX) identifies which end to place the positive end.
10. Tweezers, a low power microscope, and lots of lighting can help a lot when handling, placing, and soldering surface mount components.
11. Use small diameter, 0.022" or less, silver bearing solder, and a similarly small soldering iron tip. Only the ends of components being soldered to the ground plane will require the greater heat from a larger tip. Keep soldering iron tips clean & tinned.
12. Pay particular attention to location and orientation of the ICs before they are soldered down.
13. Take your time and work for short periods at a stretch. The small components put a strain on the eyes.
14. Building by "functional islands" will, I think, ease the task.
15. Some of the clearances between lands on the bottom side and the ground plane are very tight - again, to maximize ground plane integrity. These can be bridged easily if one is not careful.
16. During my build, I combined frequent visual inspections with continuity checks at most points and particularly any tight clearance spots.
17. Use a low voltage & low current continuity checking. These are common on newer digital multi-meters. Older analog ohmmeters can damage ICs, so make sure your's will not, before using it for continuity checking.
18. Don't forget the nine backside wire "ground to ground" jumpers, designated W1-W9 in a footnote on page 1 of the schematics. Use solid AWG #30, teflon insulated wire. Their locations aren't shown on the schematic but are shown on the layout drawings. If you look closely, you can probably see them on the backside photo. I put these in to maximize the RF integrity of the ground plane by bridging across the major disruptions to the ground plane at decoupling cap & overflow land sites.
19. Checking the R & C component values before installation can save a lot of headaches later. Do this carefully though as the component can be sent flying while pressing test leads against it.
20. I suggest the following procedure for placing components. Start with a component on the schematic. Identify it completely using the parts list. Find it on the layout & photos if possible. Find the component itself. Tin one lead on it. Use a low power microscope as needed. Position the component with tweezers on the board. Double-check its location. Re-flow solder the tinned lead to the board. Continue with the rest of its leads. Yellow mark it on the schematic, the parts list, and the layout drawing. (When everything is yellow-marked, you're done!)
21. These small components tend to disappear or get sneezed away on the workbench. Only take out the one you are placing.
22. For coax cable connections to the PCB, I suggest the following. Prepare a 0.25" long, 0.125" OD, brass or copper tube to be used as a shim. It also provides an interface that is easier to solder & unsolder the coax shield. Sand the shim down as needed to fit into the hole on the PCB. Tin just the coax end. Slid the shim into the hole just a little higher than flush with the component side and soldered it in place. Prepare the coax so the braid is fanned out like a disk, tin it, and trim it to be just long enough to just fold over the end of the brass/copper tube. Also tin its center conductor. Slide the coax thru the shim. Support it so it is perpendicular to the PCB while soldering the shield to avoid shorting the center to the shield. Re-flow solder the braid to the shim. Fold the braid down over the shim walls while soldering. Then solder the coax center conductor to the PCB pad with a short solid AWG #30 teflon wire, routing the wire flat against the board. Here are two close-up pictures of the shim terminated coax:



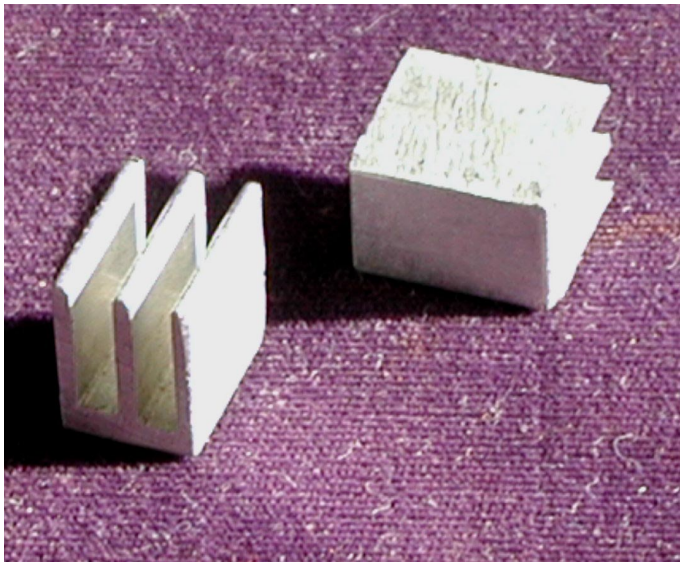


This coax termination technique can also be seen in the earlier PCB photos and in the higher resolution photos in the VNA PCB 'Build Info' PDF file.
23. Double check components and re-check the board for shorts, particularly on the external power pins before powering it up. Double-check the voltages and polarities to be applied to the board. After powering up, check the DC voltages noted on the schematics. Then proceed to the initial software tests per Part 3.

General Build Notes

In addition to the comments in the Enclosure section, here are some additional considerations:

1. The DDS modules are the major heat sources on the VNA PCB. To divert the heat away from the detector as much as possible, I have used heat sinks on the DDSs as seen here:



These heat sinks are used with a standard thermal compound between them and the DDS module top surfaces. As I do not have a finished enclosure, I have yet to work out a good way to secure these heatsinks in place. I prefer to not permanently attach these to the DDS modules, in case the modules have to be replaced. Providing a good thermal path between the DDS modules and the enclosure exterior would be best, but probably difficult. These heat sinks are not mandatory, but may help reduce warm-up time and subsequent detector drift.

2. Consider making the SMA connector holes "D" shaped to prevent them from rotating during use.

**Acknowledgements**

I wish to acknowledge and thank the following individuals for their contributions to all aspects of this project. Everyone contributed in ways to too numerous, but here are a few highlights in roughly chronological order.

First is Bob Stedman, K9PPW, now sadly passed on, who was there for my first VNA related e-mail in Oct. 1997 titled "Baluns & A Cheap Network Analyzer." Bob was quick to offer many helpful thoughts on the VNA and many other topics as well. His counsel and friendship will be missed.

Next is Bill Craddock, WB4NHC. Bill, unlike Bob, had to put up with my early VNA related ramblings in person, and that helped enormously in clarifying some early ideas.

I was introduced to Bill Carver, W7AAZ, by Steve Weber, KD1JV, in connection with another project. Bill steered me toward using the PC parallel port, which greatly improved the VNA's flexibility, programmability and performance. Bill also suggested a simple yet elegant way to extend the frequency range of the VNA into the VHF and UHF range. This resulted in the "Synchronous Common LO up/down mixing" frequency entry mode that is available in many of the programs. Bill also recently suggested providing the user with the option of naming the test data files - a feature that has already proved to be worthwhile. Bill was VNA builder #3.

Bill Carver introduced me to Harold Johnson, W4ZCB. Harold was VNA builder #2 and guinea pig #1. Harold, armed with his adventurous spirit, willing constructed his VNA with the least amount of available documentation. Harold also suggested the idea of re-usable calibrations in the software. I initially resisted implementing this, but it is now a feature I would not do without. Harold also refers to his VNA as "the lab in a box."

Harold Johnson and Bill Carver both have also provided a great deal of assistance, in general, by being the primary beta software testers. Harold has also provided a great deal of data that has 'sanity checked' VNA test results.

Bill Carver introduced me to Chip Owens, NW0O. Chip provided the other half of a reflection correlation activity using a commercial VNA, as summarized in Part 1. This was enormously valuable for the correlation itself as well as the measurements of various homebrew SMA terminations.

Harold introduced me to Jim Tonne, WB6BLD. Jim graciously provided a wonderful jumpstart in the design of the Smith Chart that appears in the reflection test program. That also provided the impetus to provide graphics in the other programs as well.

Harold also introduced me to Ian White, G3SEK. Ian is VNA builder #4. Ian provided the wonderful annotated images of the VNA PCB that make up for the lack of a component silkscreen. Ian also built & tested a modified master oscillator as well as contributing to the text in several places.

Throughout all of this and most important is my wife, Kathy, K2KAK. Kathy has tolerated the seemingly endless hours that I put into this project.

Notes

Clicking on a URL below with an active Internet connection, in most cases, will either bring it up a document in your web browser if you have the Adobe plug-in for PDF files, or initiate a download for ZIP files. If any documents cannot be found (the web is a dynamic place), please contact me by e-mail.

1. The program used for all PCB artwork generation, including the main VNA PCB, can be found at:
   **http://www.expresspcb.com/**
   In addition, the software can be used to purchase the main VNA PCB (Mini-board) from ExpressPCB
2. Detailed build information for the VNA PCB can be found at:
   **http://users.adelphia.net/~n2pk/VNA/VNA_PCB_V1B_Build_Info.zip**
3. The datasheet for the SN74ACT1284 parallel port buffer can be found at:
   **http://focus.ti.com/lit/ds/symlink/sn74act1284.pdf**
4. The datasheet for the 74AC74SC dual D-type flip-flop can be found at:
   **http://www.fairchildsemi.com/ds/74/74AC74.pdf**
5. A description of metastability can be found at:
   **http://www-s.ti.com/sc/psheets/sdya006/sdya006.pdf**
6. There are many typographic errors in the equations in Reference 5. But applying its equation 6 twice to its Figure 10 & based on **continuous** frequency programming with ADC reads in the current VNA detector (#1), a frequency programming error is estimated to occur once every 20.6 years. With a 100X increase in frequency rate using the future real-time detector (#2), it's once every 75 days. This calculation also does not include the effects of probable similar synchronization of the FQ_UD line internal to the AD9851s. If present, that would increase the time interval between programming failures even further.
   An accelerated test, doing just DDS frequency programming & looking for phase errors, was also run on the VNA at 150 MHz. In this test, 5000 DDS programs/sec could be done. **No** phase errors occurred in 24,000,000 frequency programs. That test equates to about 40 days of **continuous** DDS programming with data reads of the current VNA detector. Since no errors were found, the test time should be increased to get at least 1 or preferably 2 errors to get a meaningful estimate of MTBF.
7. Jitter & phase noise info for the Valpey-Fisher and Fox oscillator can be found at:
   **http://www.valpeyfisher.com/Data/HomePageTechns/Docs/VF(0530E).pdf**
   **http://www.valpeyfisher.com/Data/DescriptionFiles/VF(B5FB3).pdf**
   **http://www.foxonline.com/pdfs/JITO-2_brochure.pdf**
8. The datasheet for the Analog Devices AD9851 DDS can be found at:
   **http://www.analog.com/UploadedFiles/Data_Sheets/41539448AD9851_c.pdf**
9. Ed Wetherhold, "Second-Harmonic-Optimized Low-Pass Filters," QST, Feb. 1999, pp 44-46.
10. The datasheet for the Analog Devices AD8041 wideband amplifier can be found at:
    **http://www.analog.com/UploadedFiles/Data_Sheets/36627127014387AD8041_b.pdf**
11. The datasheet for the Panasonic ferrite beads can be found at:
    **http://www.panasonic.com/industrial/components/pdf/ex005_exc_cl_ml_3b_dne.pdf**
12. The datasheet for the Motorola (now called ON Semiconductor) MC1496 balanced modulator/demodulator and a related application note can be found at:
    **http://www.onsemi.com/pub/Collateral/MC1496-D.PDF**
    **http://www.onsemi.com/pub/Collateral/AN531-D.PDF**
    A similar part is made by National Semiconductor, the LM1496, but is listed as discontinued. The datasheet can be still found at:
    **http://www.national.com/ds.cgi/LM/LM1496.pdf**
13. The datasheet for the Linear Technology LT1677 op amp can be found at:
    **http://www.linear-tech.com/pdf/1677f.pdf**
14. The datasheet for the Linear Technology LTC2410 ADC can be found at:
    **http://www.linear-tech.com/pdf/2410fs.pdf**
15. The datasheet for the Linear Technology LT1460-2.5 voltage reference can be found at:
    **http://www.linear-tech.com/pdf/146025fs.pdf**
16. The datasheet for the National LP2951 voltage regulator can be found at:
    **http://cache.national.com/ds/LP/LP2950.pdf**
17. The datasheet for the Microchip TC7662B DC-DC voltage converter can be found at:
    **http://www.microchip.com/download/lit/pline/analog/power/charpump/21469a.pdf**
18. The datasheet for the National LM79L05 negative voltage regulator can be found at:
    **http://cache.national.com/ds/LM/LM320L.pdf**
19. Detailed build information for the homebrew master oscillator can be found at:
    **http://users.adelphia.net/~n2pk/VNA/VNA_MO_V1B_Build_Info.zip**
20. John Stephensen, "A Stable, Low-Noise Crystal Oscillator for Microwave and Millimeter-Wave Transverters," QEX, Nov/Dec 1999, pp 11-17.
21. Detailed build information for the master oscillator test board can be found at:
    **http://users.adelphia.net/~n2pk/VNA/VNA_MO_Test_Board_V1B_Build_Info.zip**
22. The ratio of average to power supply voltage approximation for oscillator duty cycle depends on AC logic output levels being essentially tied to ground on the down level and to the power pin (Vdd) on the up level, and the threshold for the driven circuitry being at Vdd/2.
23. Some Littlefuse info:
    **http://www.littlefuse.com/PDFs/EDG_Cat/Fuseology.pdf**
24. A useful survey of RF connectors and their care can be found at:
    **http://www.micromanipulator.com/A1013703.PDF**
25. The effects of improper connector mating can be seen in some photos at:
    **http://www.picosecond.com/objects/5510V%20SPEC-4040076.pdf**
26. SMA torque spec and wrench info can be found at:
    **http://www.maurymw.com/Prdln2/trqwnchs/TorqWrnchs.htm**
27. The Hammond 1458G5 enclosure can be found at:
    **http://www.hammondmfg.com/pdf/9c2pg76.pdf**
28. Detailed build information for the T1-6T bridge can be found at:
    **http://users.adelphia.net/~n2pk/VNA/T1-6T_Bridge_V1A_Build_Info.zip**

29. 3.5 mm calibration kit data can be found on page 53 of:
    **http://cp.literature.agilent.com/litweb/pdf/85052-90078.pdf**
    How to use the data can be found at:
    **http://cp.literature.agilent.com/litweb/pdf/5956-4352.pdf**
30. 0.1% surface mount resistors are available from Digi-Key as follows:
    100-Ω, 0603: P100YCT-ND
    200-Ω, 0603: P200YCT-ND
    100-Ω, 0805: P100ZCT-ND
    200-Ω, 0805: P200ZCT-ND
31. A drawing of the Amphenol 901-144-8RFX female SMA connector (available at Digi-Key) can be found at:
    **http://65.244.34.140/Customer%20Outline/C901-144-8RFX.pdf**
32. A drawing of the Amphenol 901-9895-RFX male SMA connector (available at Digi-Key) can be found at:
    **http://65.244.34.140/Customer%20Outline/C901-9895-RFX.pdf**