Contents

This document provides the fast detector hardware update to the original single detector N2PK VNA as well as dual fast detector Expanded N2PK VNA. VE3IVM's PCBs already incorporate the fast detectors. While Figs 1-4 are applicable to the VE3IVM PCBs with additional LO DDS changes noted at his website, the build notes here are only to be used with the original ExpressPCB PCB. With the later addition of the S-Parameter Test Set and new software, the Expanded N2PK VNA will support all of the features shown at:

http://n2pk.com/VNA/FastADCOverview.html

The S-Parameter Test Set is not required to take advantage of dual detectors.

The pages that follow are:

Notes:

Figs A-D are intended to aid a potential builder in deciding which VNA configuration best meets requirements.

PCB #1 contains the VNA master oscillator, DDS sources, Detector #1, voltage regulators, and the parallel port interface for the DDSs and Detector #1.

PCB #2 is the same layout, but is only populated with Detector #2, voltage Regulators, and the parallel port interface for Detector #2.

The photos highlight Detector #2 new components, but can be used for Detector #1 on PCB #1.

Fig. A. N2PK VNA Block Diagram - Single Detector

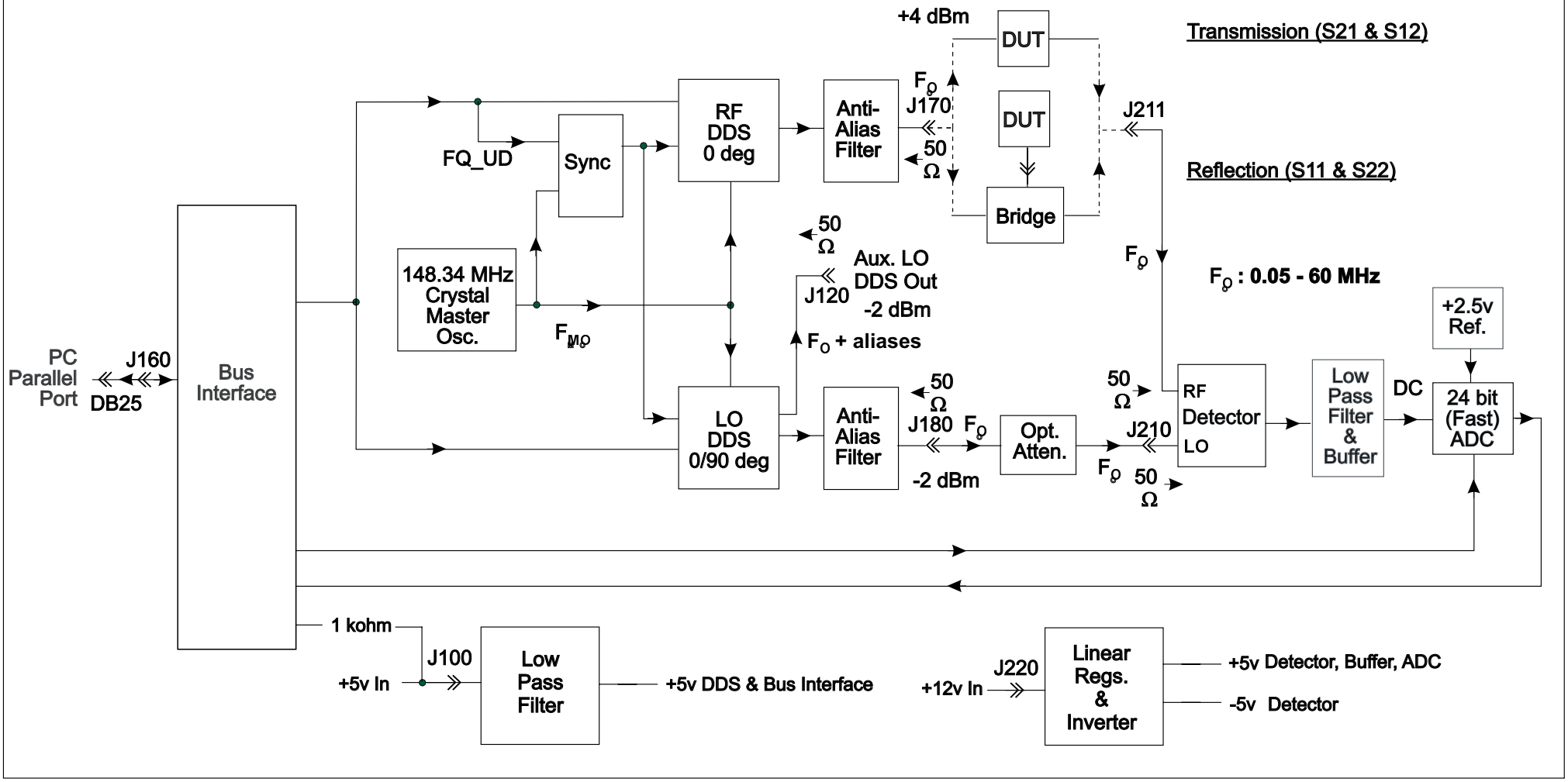


Fig. B. Expanded N2PK VNA Block Diagram (without S-Parameter Test Set)

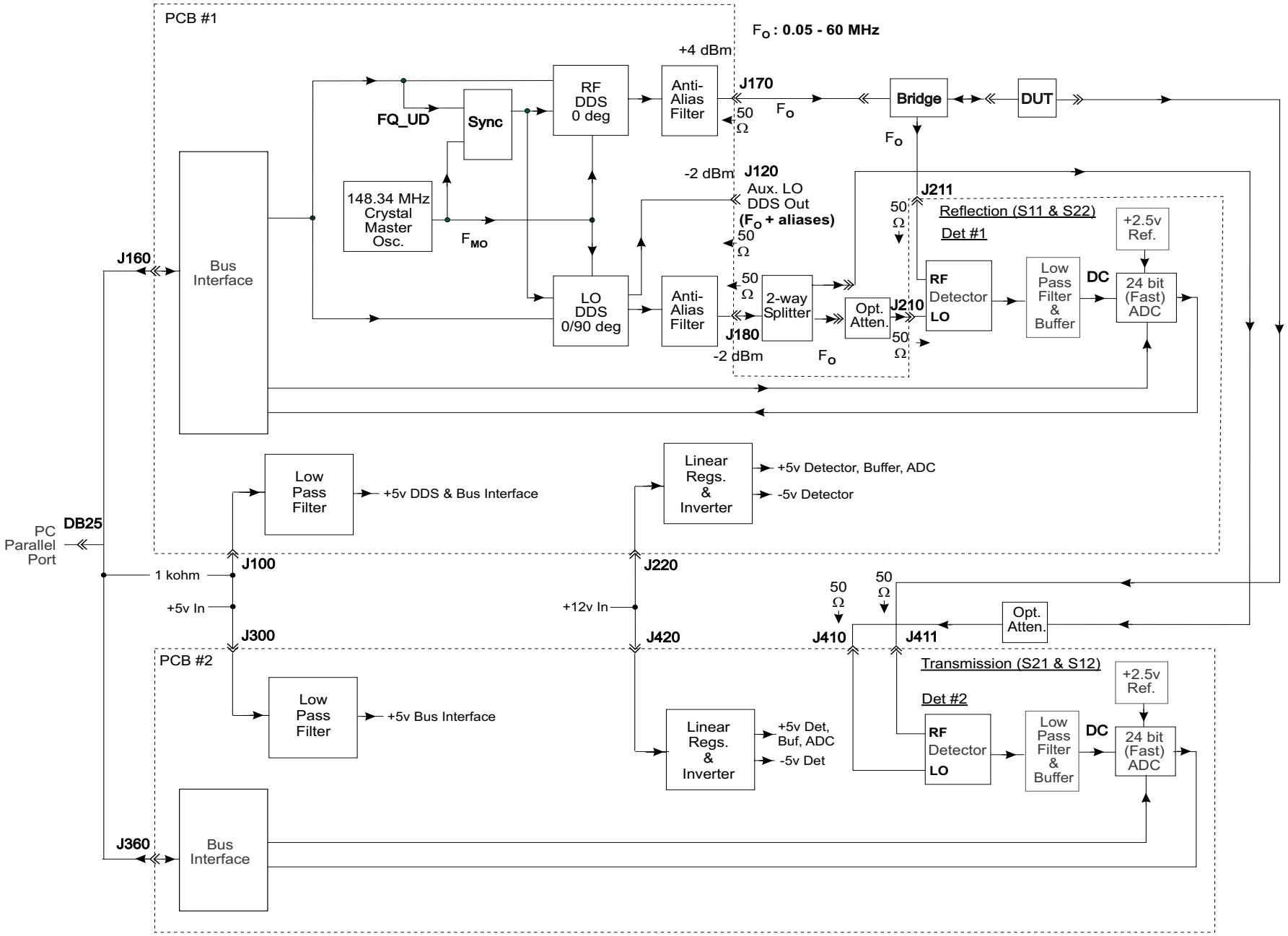


Fig. C. Expanded N2PK VNA Block Diagram (with S-Parameter Test Set)

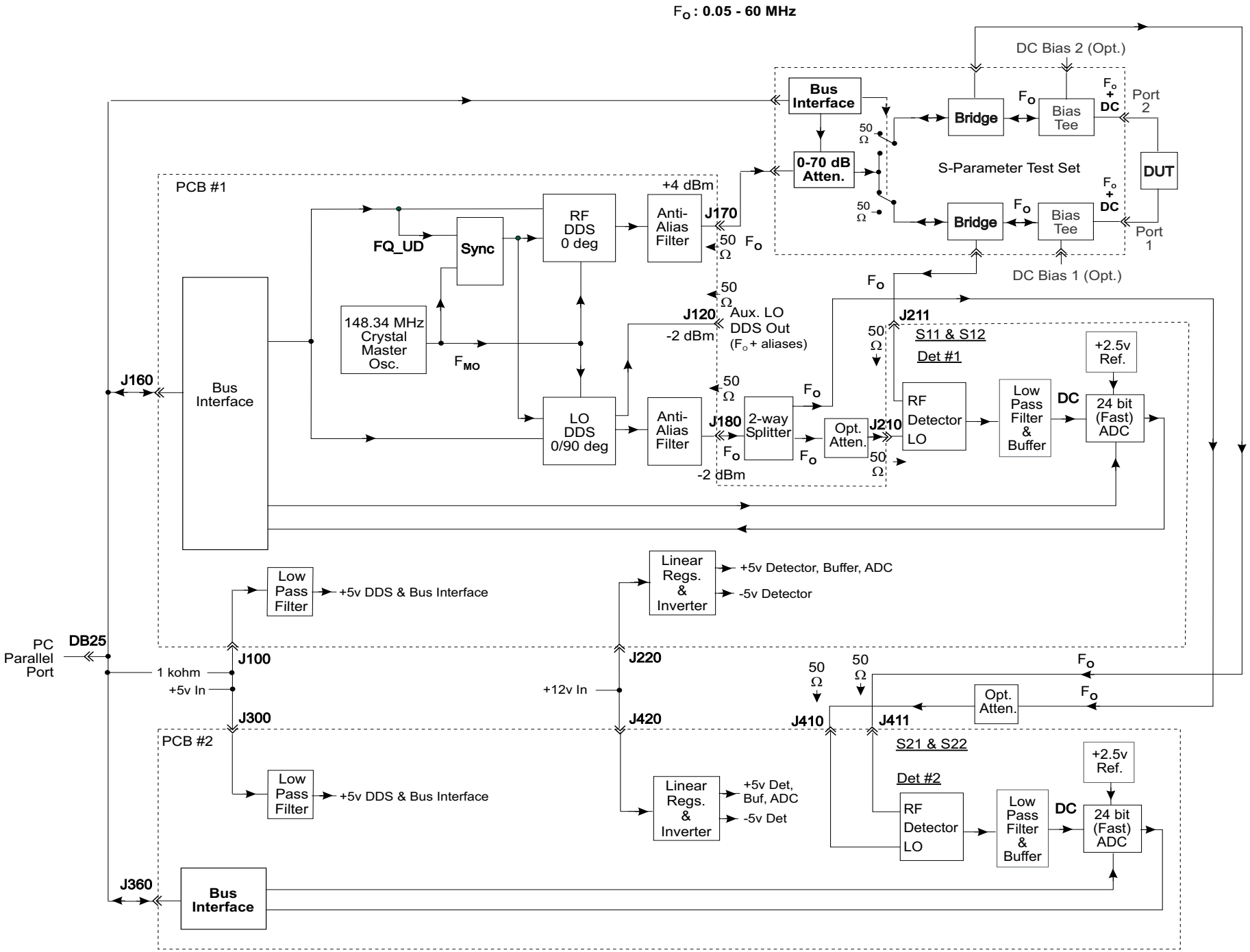
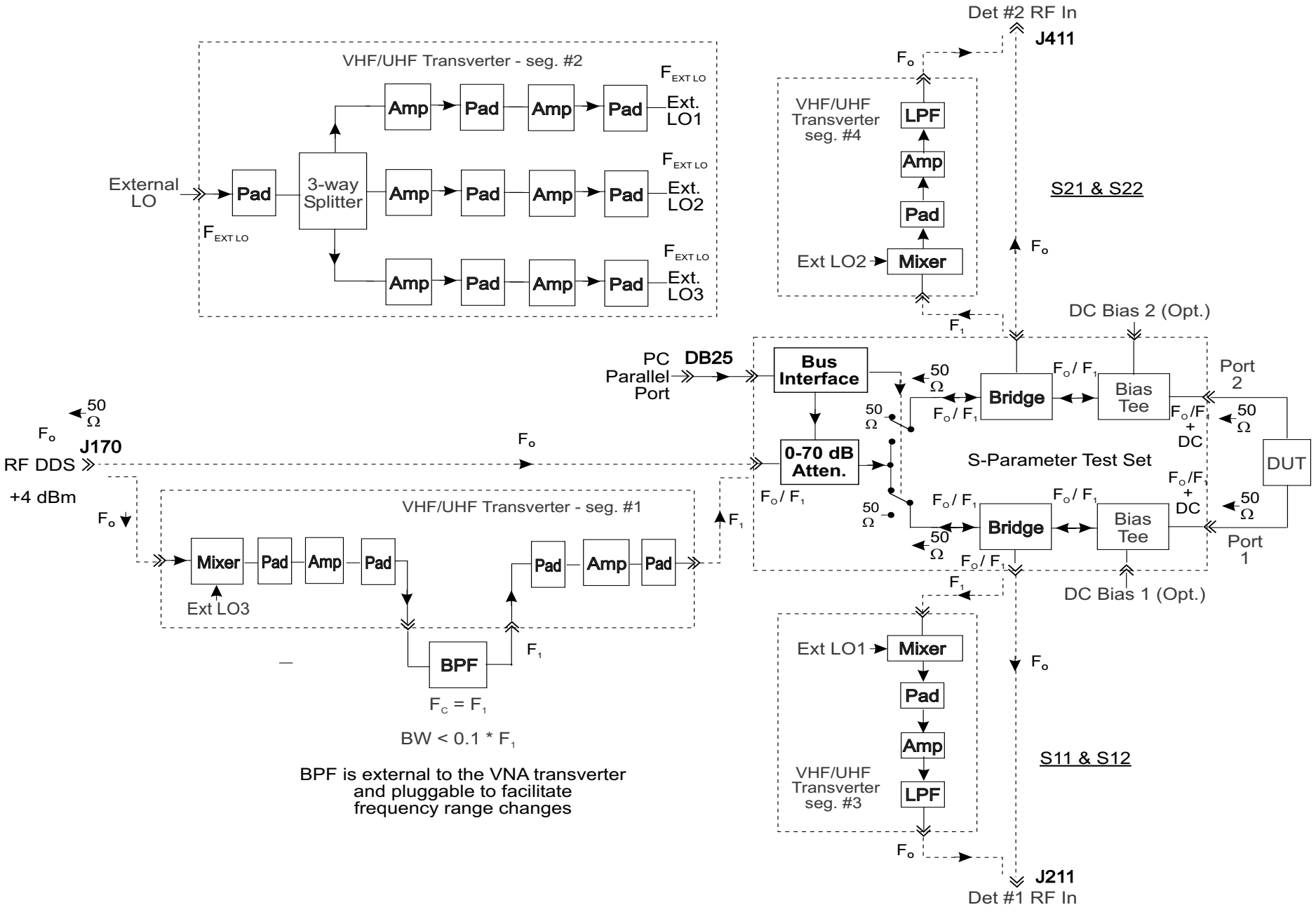


Fig. D. S-Parameter Test Set with Optional VNA VHF/UHF Transverter

F_o : 0.05 - 60 MHz **F_1 : 60 - 500 MHz, approx +/- 5% max range around F_1 for each "BPF"** $F_{EXT\ LO} = F_1 +/- F_o$



BPF is external to the VNA transverter and pluggable to facilitate frequency range changes

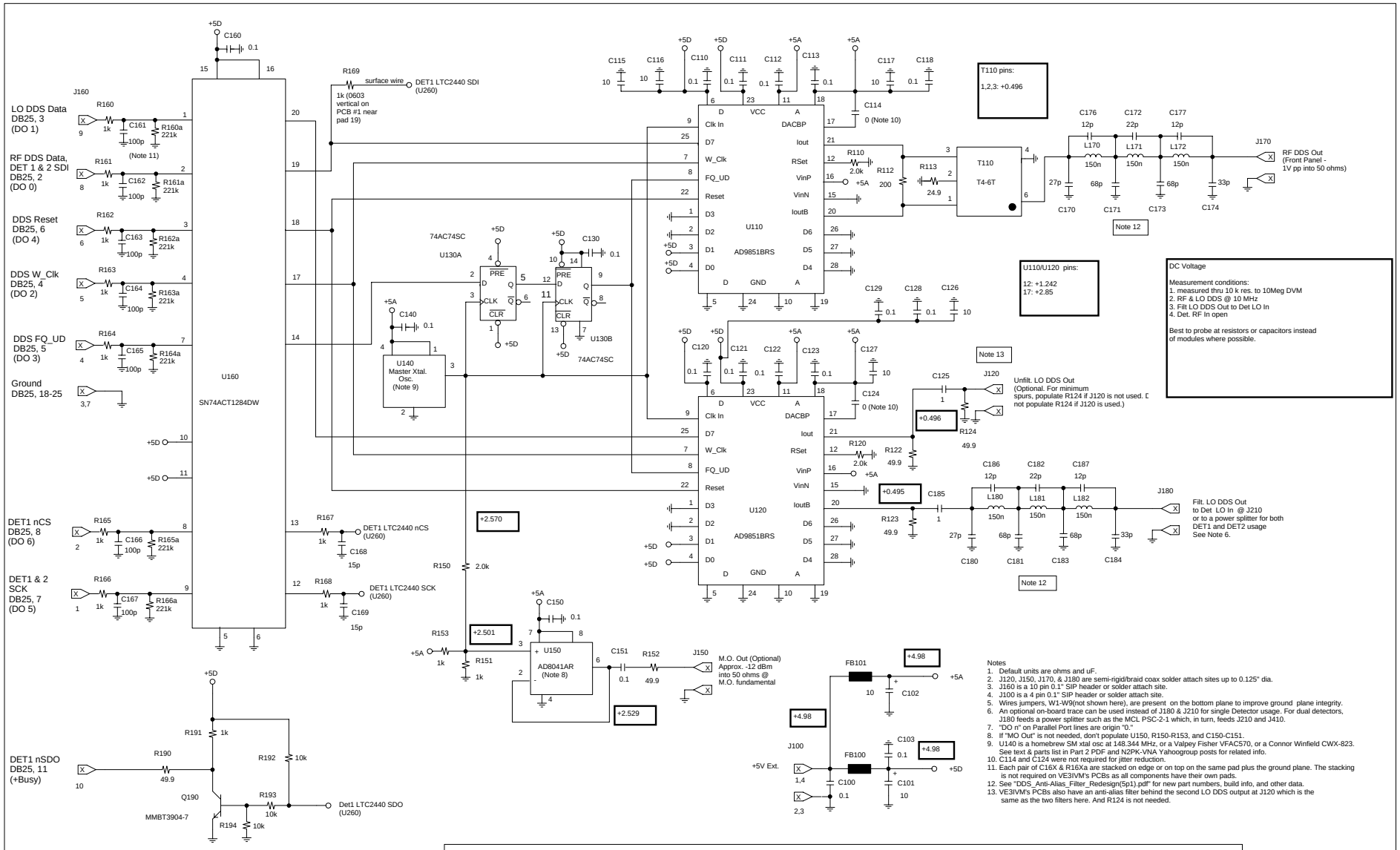


Figure 1. N2PK Fast VNA PCB #1 Schematic - DDS Sources

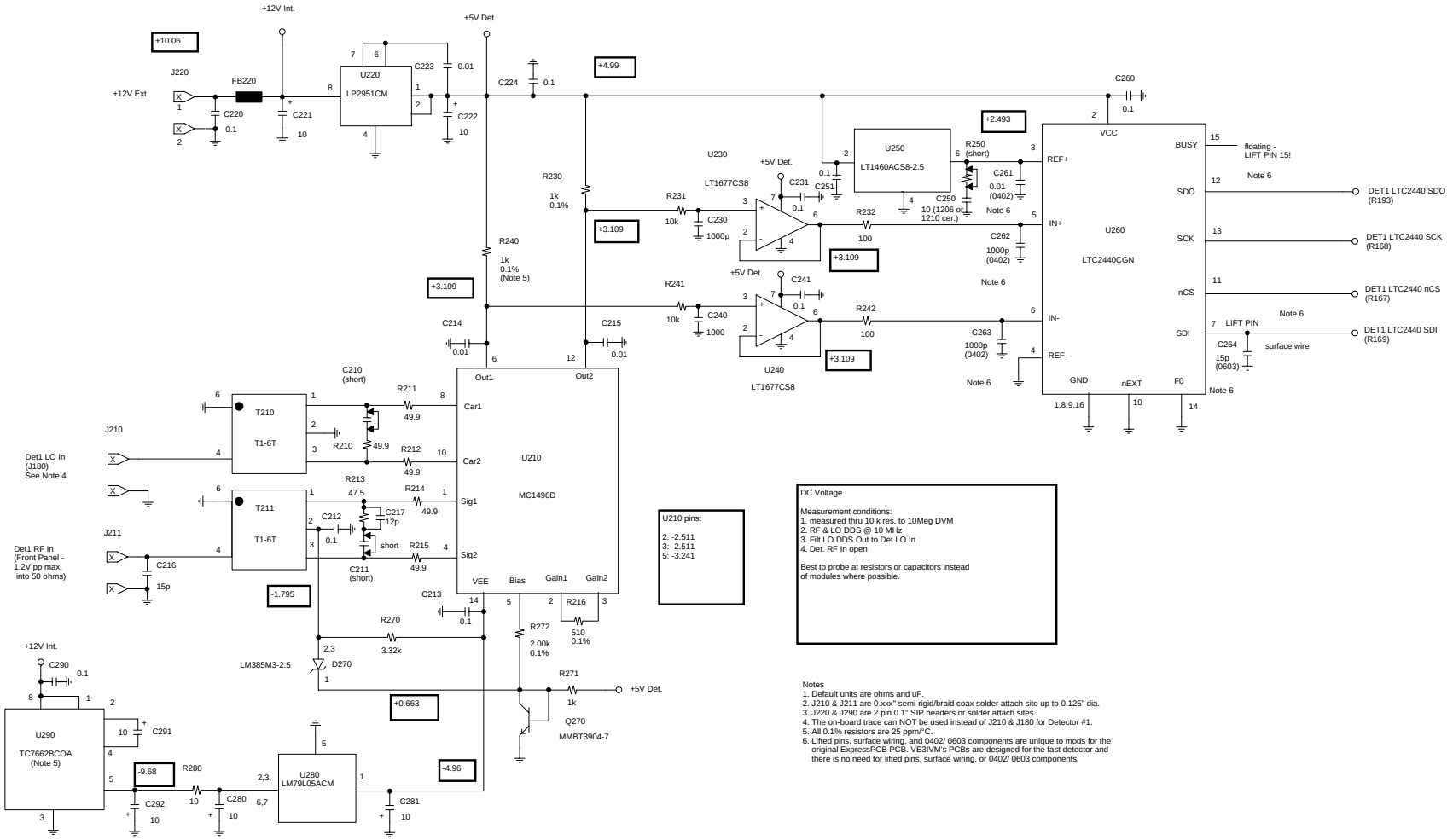


Figure 2. N2PK Fast VNA PCB #1 Schematic - Detector #1

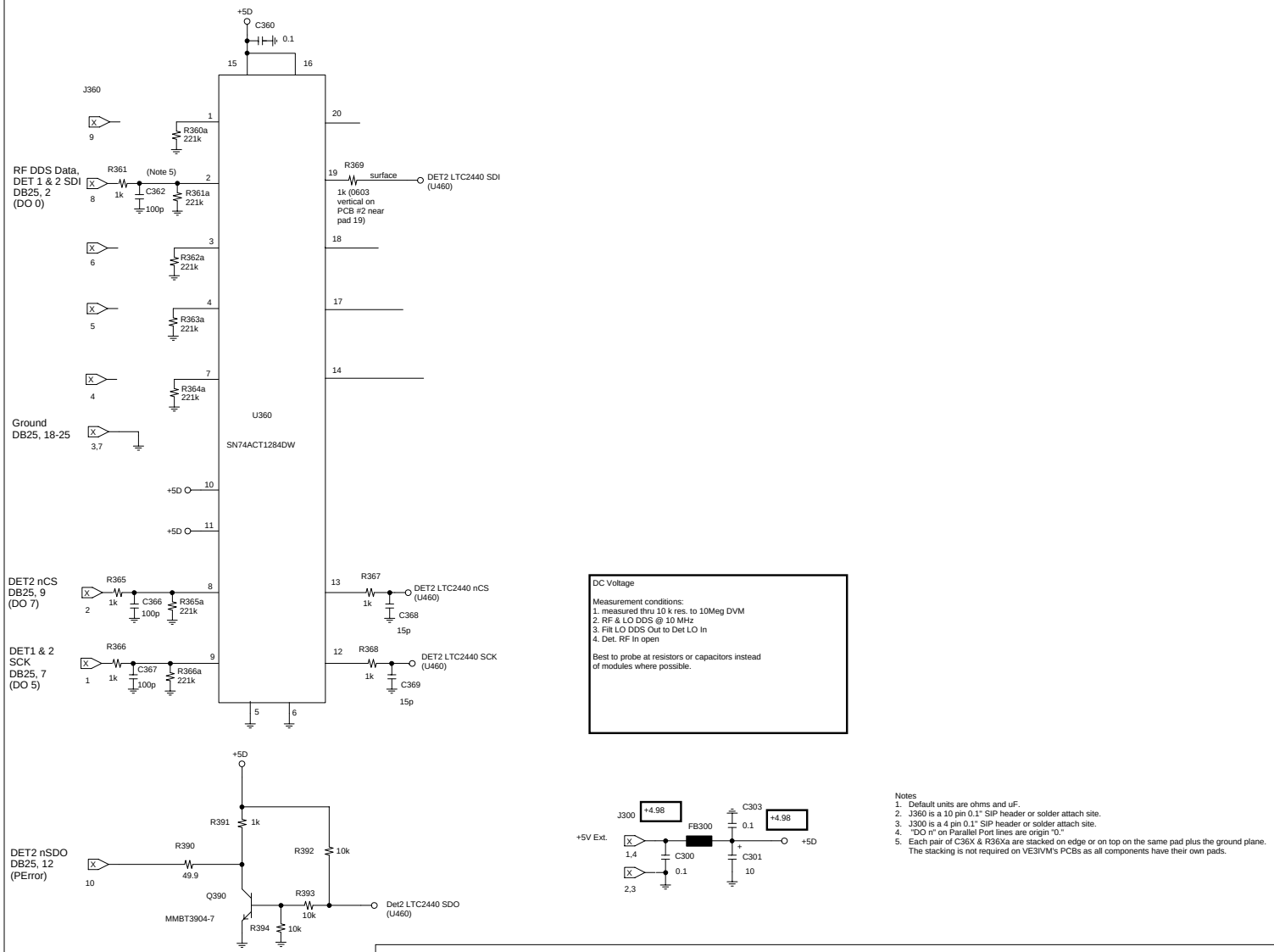


Figure 3. N2PK Fast VNA Detector #2 PCB #2 Schematic - Parallel Port Interface

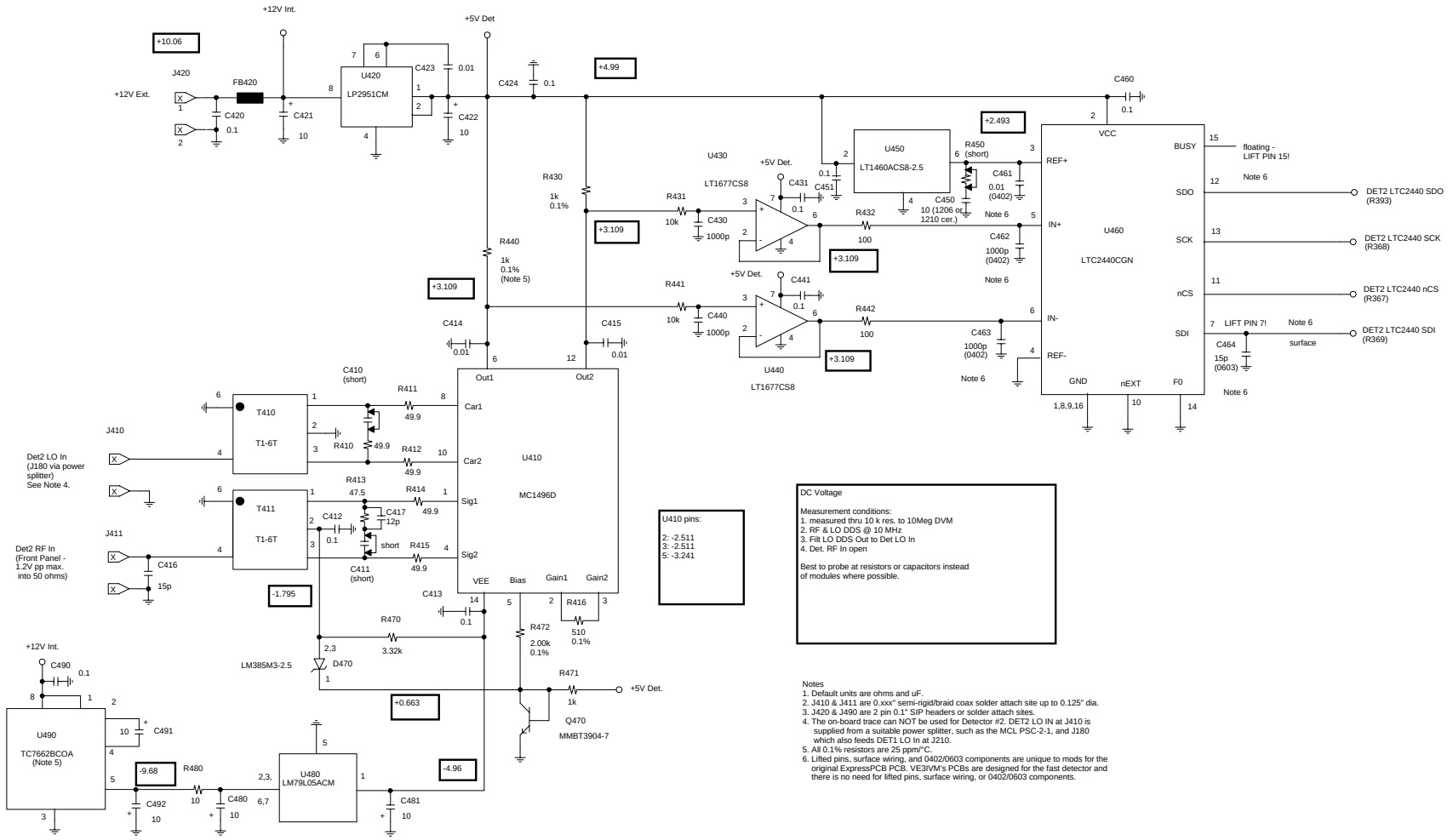


Figure 4. N2PK Fast VNA Detector #2 PCB #2 Schematic - Detector #2

Fast Detector #1 Build Notes

Fast Detector #1 component changes, additions, deletions are noted here with respect to parts designated for the original "Slow" Detector #1 in the "Part 2" PDF. Refer to the Part 2 PDF for the complete parts list as only the changes, additions, and deletions are noted here.

Item	Designation	Type	New Value	Package	Digikey PN(s)
1	R169	Add	1 k	0603	P1.00KHCT-ND
2	R250	Del	0/short	-	-
3	C250	Chg	10 u	1206/1210	PCC1940CT-ND/PCC2169CT-ND
4	C261	Add	0.01 u	0402	PCC2270CT-ND
5	C262	Add	1000 p	0402	PCC1721CT-ND
6	C263	Add	1000 p	0402	PCC1721CT-ND
7	C264	Add	15 p	0603	PCC150ACVCT-ND
8	C214	Chg	0.01 u	0805	PCC103BNCT-ND
9	C215	Chg	0.01 u	0805	PCC103BNCT-ND
10	C230	Chg	1000 p	0805	PCC102BNCT-ND
11	C240	Chg	1000 p	0805	PCC102BNCT-ND
12	R232	Chg	100	0805	P100CCT-ND
13	R242	Chg	100	0805	P100CCT-ND
14	U260	Chg	LTC2440CGN	SSOP-16	LTC2440CGN-ND

1. The fast (LTC2440) ADC can be used on either Detector #1 or #2 or both. The PCB modifications are identical. The connections to the DB25 determine whether it is Detector #1 or Detector #2.
2. See photos for locations of added components. Also refer to website docs if needed for drawings of Detector #1 components.
3. R169 stands up vertically off the PCB on pad near U160, pin 19.
4. C264 attaches to U260 (gnd) pads 9 & 10 & lays flat on the PCB.
5. When U260 is installed, lift pins 7 and 15 so they do not contact the pads below.
6. Surface wire from R169 to C264 to U260 pin 7. One wire with an insulation gap @ C264 is easiest. Use hot melt glue wire hold-downs, as shown in the photo.
7. C250 in the photo is the 1210 PN and one lead bridges the original location for R250. If C250 is the 1206 PN, then the bridge is not required since C250 can be directly connected only to U250, pin 6. The other side of C250 is grounded.
8. The schematics for PCB #1 show all components needed, while the photos show only those components that are required for PCB #2 - i.e. for Detector #2. PCB #1, which contains Detector #1, would be populated with additional components per the parts list in Part 2 of the VNA documentation and the schematics here.

Fast Detector #2 Build Notes

Fast Detector #2 component changes, additions, deletions are noted here with respect to parts designated for the original "Slow" Detector #1 in the "Part 2" PDF. The format here for Detector #2 under "Designation" is "new / old". A study of all schematics included here should make this clear. Refer to the Part 2 PDF for the complete parts list as only the changes, additions, and deletions are noted here.

Item	Designation	Type	Value	Package	Digikey PN(s)
1	R369 / R169	Add	1 k	0603	P1.00KHCT-ND
2	R450 / R250	Del	0	-	-
3	C450 / C250	Chg	10 u	1206/1210	PCC1940CT-ND/PCC2169CT-ND
4	C461 / C261	Add	0.01 u	0402	PCC2270CT-ND
5	C462 / C262	Add	1000 p	0402	PCC1721CT-ND
6	C463 / C263	Add	1000 p	0402	PCC1721CT-ND
7	C464 / C264	Add	15 p	0603	PCC150ACVCT-ND
8	C414 / C214	Chg	0.01 u	0805	PCC103BNCT-ND
9	C415 / C215	Chg	0.01 u	0805	PCC103BNCT-ND
10	C430 / C230	Chg	1000 p	0805	PCC102BNCT-ND
11	C440 / C240	Chg	1000 p	0805	PCC102BNCT-ND
12	R432 / R232	Chg	100	0805	P100CCT-ND
13	R442 / R242	Chg	100	0805	P100CCT-ND
14	U460 / U260	Chg	LTC2440CGN	SSOP-16	LTC2440CGN-ND

1. The fast (LTC2440) ADC can be used on either Detector #1 or #2 or both. The PCB modifications are identical. The connections to the DB25 determine whether it is Detector #1 or Detector #2.
2. See photos for locations of added components. Also refer to website docs if needed for drawings of Detector #1 components.
3. R369 stands up vertically off the PCB on pad near U360, pin 19.
4. C464 attaches to U460 (gnd) pads 9 & 10 & lays flat on the PCB.
5. When U460 is installed, lift pins 7 and 15 so they do not contact the pads below.
6. Surface wire from R369 to C464 to U460 pin 7. One wire with an insulation gap @ C464 is easiest. Use hot melt glue wire hold-downs, as shown in the photo.
7. C450 in the photo is the 1210 PN and one lead bridges the original location for R450. If C450 is the 1206 PN, then the bridge is not required since C450 can be directly connected only to U450, pin 6. The other side of C450 is grounded.
8. The schematics and photos show only those components that are required for Detector #2 PCB.

Planned N2PK VNA Parallel Port Assignments

DB25	Port Name	VNA Line Name	Type	Port Offset(1)	Register Bit(2)
+ 1	Strobe*	Test Set Sw(2 rx)	Out	2	n0
2	D0	RF DDS Data	Out	0	0
2	D0	DET1 SDI	Out	0	0
2	D0	DET2 SDI	Out	0	0
3	D1	LO DDS Data	Out	0	1
4	D2	DDS W_CLK	Out	0	2
5	D3	DDS FQ_UD	Out	0	3
6	D4	DDS Reset	Out	0	4
7	D5	DET1 SCK	Out	0	5
7	D5	DET2 SCK	Out	0	5
8	D6	DET1 nCS(4)	Out	0	6
9	D7	DET2 nCS(4)	Out	0	7
10	ACK*	Unused	In	1	6
11	BUSY	DET1 nSDO(4)	In	1	n7
12	PError	DET2 nSDO(4)	In	1	5
+13	Select	VNA Present(5)	In	1	4
+14	AUTOFD*	Atten0	Out	2	n1
15	FAULT*	Unused	In	1	3
16	INIT*	Atten1	Out	2	2
17	SelectIn*	Atten2	Out	2	n3
18	Ground	Ground			
19	Ground	Ground			
20	Ground	Ground			
21	Ground	Ground			
22	Ground	Ground			
23	Ground	Ground			
24	Ground	Ground			
+25	Ground	Ground			

(1) Offset Register

Offset	Register
0	Data
1	Status
2	Control

(2) "n" in this column only signifies that the parallel port line is inverted from the register bit.

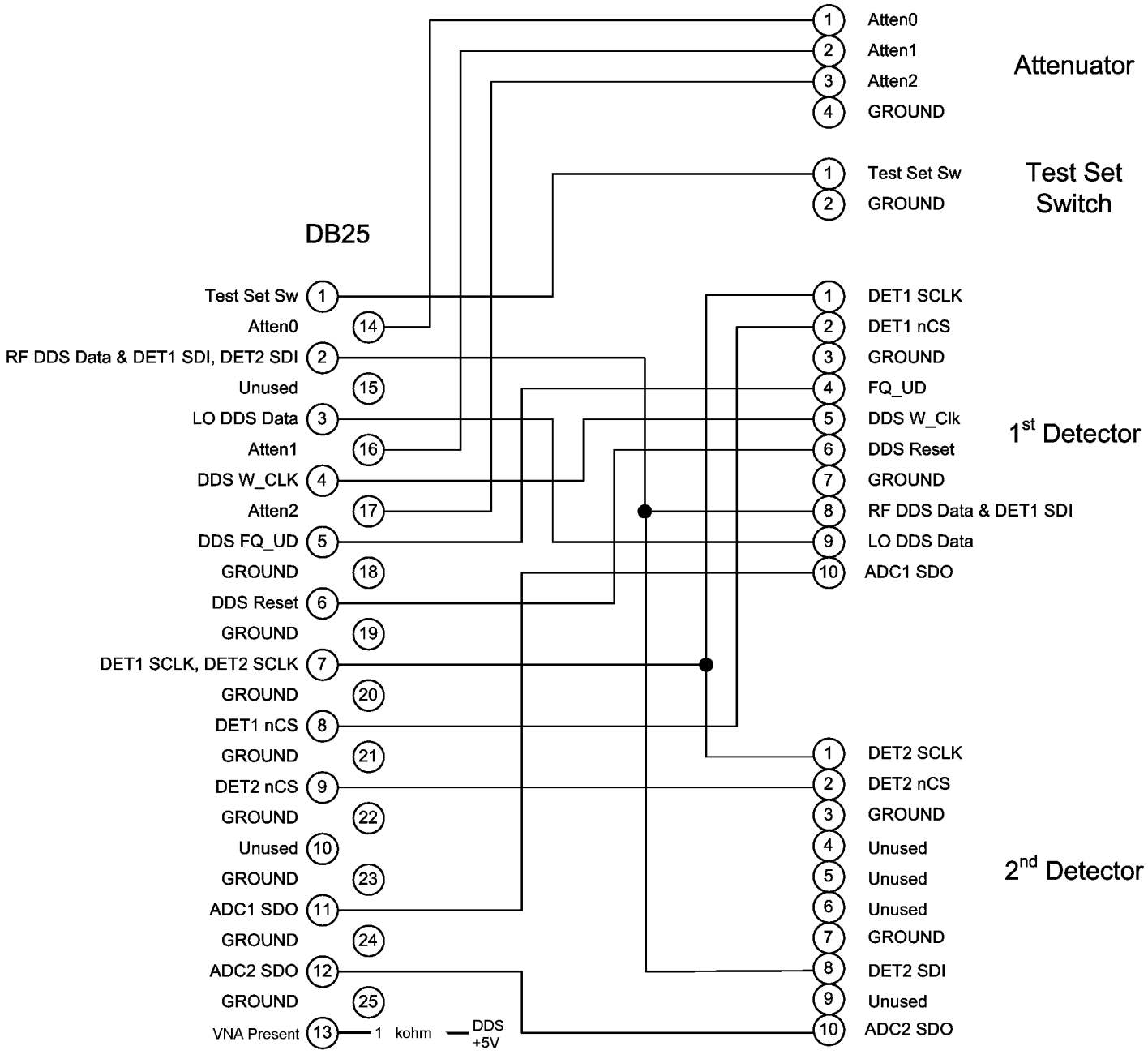
(3) "+" are DB-25 end pins

(4) Note that assignment of a particular PCB's ADC is totally controlled by which DB25 pins are used for its nCS and its nSDO. This permits the PCBs to be built identically with respect to the ADC, assuming the fast (or the slow) ADC is on both PCBs.

(5) This is +5 Vdc, used for the DDSs, thru a series 1 kohm resistor for current limiting on the parallel port. It is intended to be used by software as one way to determine if the VNA is present on the parallel port and powered up.

The designation of pins as "Unused" is not intended to preclude their future use for some yet to be defined feature or function. They are not "reserved" as there are no plans to use them at this point.

Planned N2PK VNA Parallel Port Assignments



(Connection to GROUND lines omitted for clarity)

Detector #1 and Detector #2 LO Drive Options

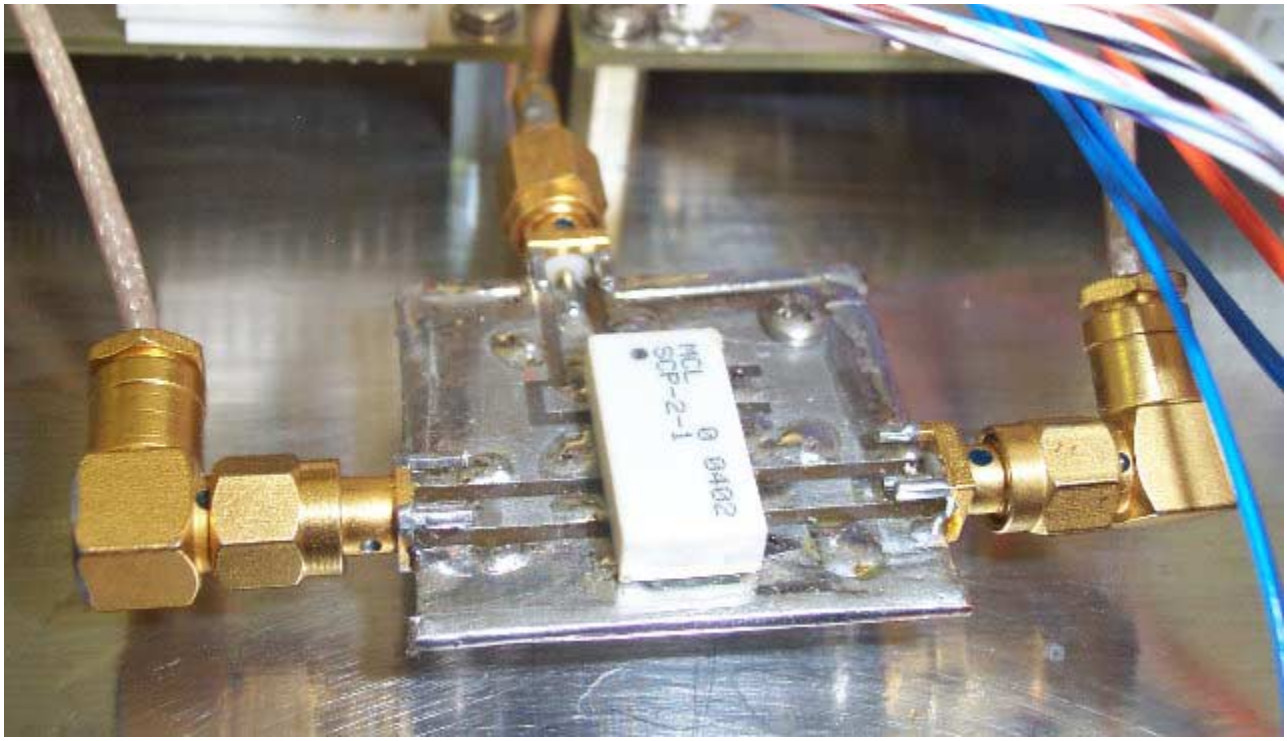
The original N2PK VNA has only one detector, while the Expanded N2PK VNA has two detectors. The LO DDS, via some combination ot its outputs at J180 and J120 must now drive the LO inputs of both detectors for proper VNA operation.

Several options are possible. Here are three that come to mind:

1. Low loss 2-way power splitter from J180 to J210 and J410. A suitable power splitter for this is the MCL SCP-2-1. The splitter "S" port is driven by J180. This incurs approx. 3.2 dB loss over the original single detector configuration.

   With the lower 3 dB frequency of 100 kHz for the SCP-2-1, accuracy may suffer some at very low frequencies vs. the original configuration.

   Here is a picture of the SCP-2-1 splitter built by Harold, W4ZCB. A DOC file of the artwork can be made available on request.



2. Resistive power splitter from J180 to J210 and J410. Three 16 ohm resistors in a wye ("Y") configuration can be used. This incurs about 6 dB loss over the original configuration. However, little or no accuracy degradation would be expected over most of the frequency range. Between 50 and 60 MHz, there may be some accuracy loss due to the reduced LO drive.

3. Separate LO paths: J180 to J210 for Detector #1 and J120 through an added anti-alias filter to J410 for Detector #2. The added anti-alias filter components are identical to those currently used for the J180 output. The new anti-alias filter should not be jury-rigged onto PCB #1 due to coupling between the filter and the near-by RF DDS components.

   The VE3IVM dual detector PCBs have the anti-alias filter components present for the J120 LO DDS Output.

This option provides essentially the same LO drive levels to each detector as the original configuration, so there should be no loss in accuracy due to drive level.

However, for the original ExpressPCB PCBs coupling at 28 MHz from the RF DDS to J120 is 16 dB higher than the coupling from the RF DDS to J180. At 28 MHz, the RF DDS signal at J180 is approx. 72 dB down from the LO DDS level. At 14 MHz, it's about 6 dB lower so I'd expect it to be about 6 dB worse at 56 MHz. Likely most of the coupling is capacitive which would make the slope 6 dB/octave.

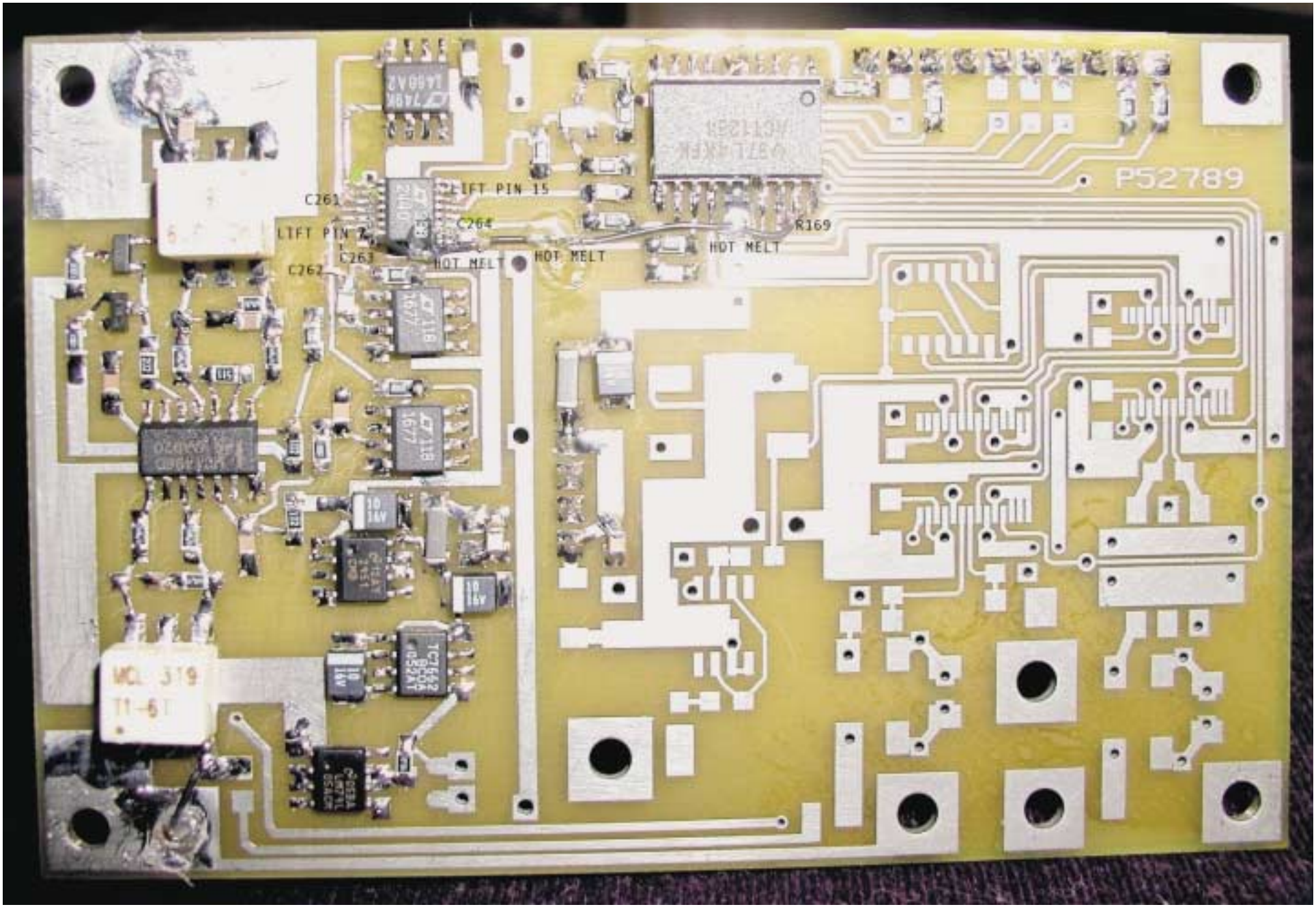
For the VE3IVM PCBs, the isolation between DDS outputs is somewhat better than for the ExpressPCB PCB.

Currently I am using either option 1 or option 2 with ExpressPCB PCBs.

Originally, it was recommended that the LO paths be made via VNA front panel coaxial jumpers to permit the optional use of attenuators for improvements to undesired harmonic mixing, where needed, as noted at:

http://n2pk.com/TestResult6.html

However, now with “Harmonic Suppression” as described in posts at the N2PK-VNA Yahoogroup, undesired harmonic mixing is virtually eliminated in fundamental mode.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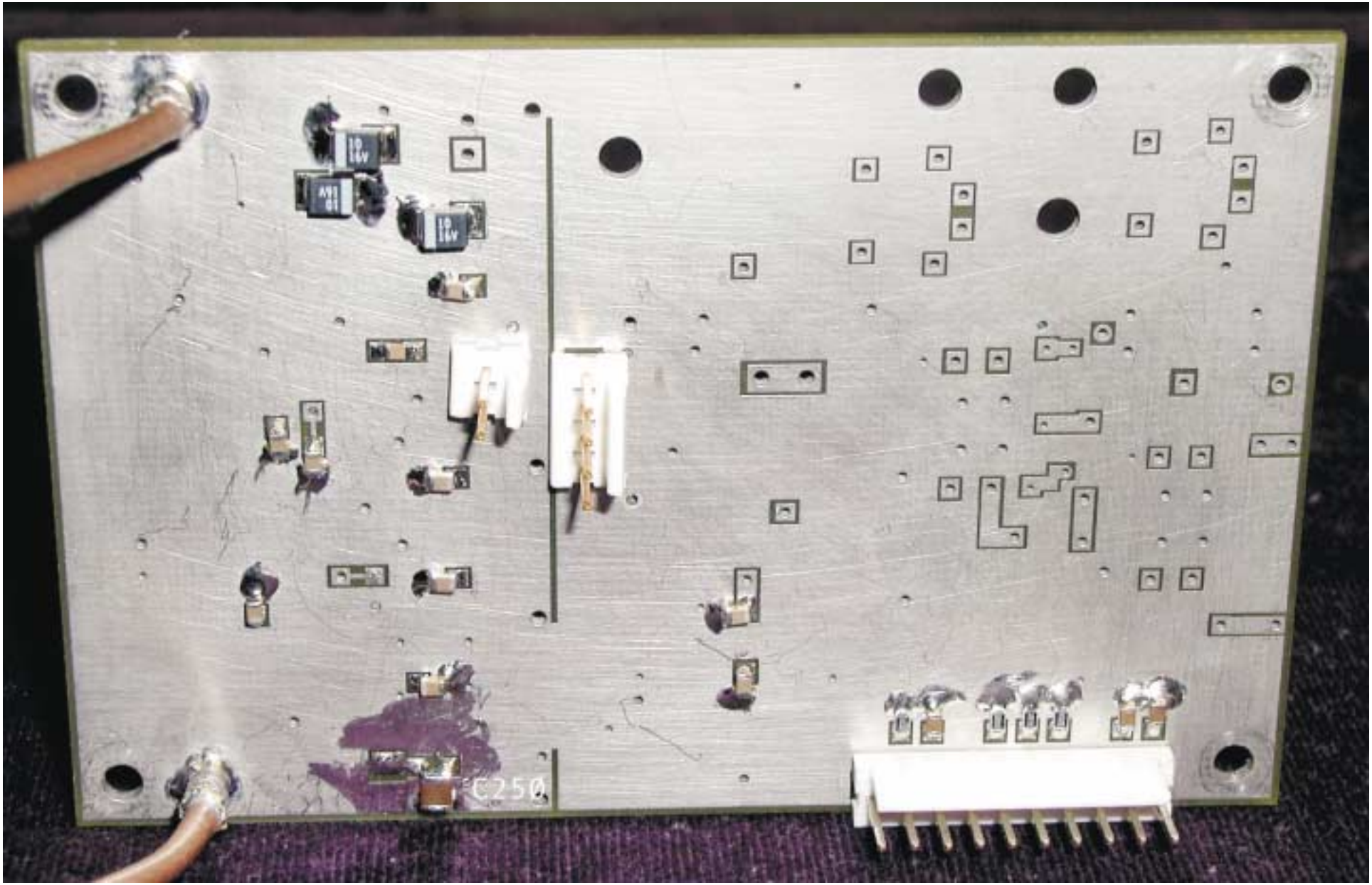
C264
LIFT PIN 2
C263
C262
HOT MELT
HOT MELT
HOT MELT
R169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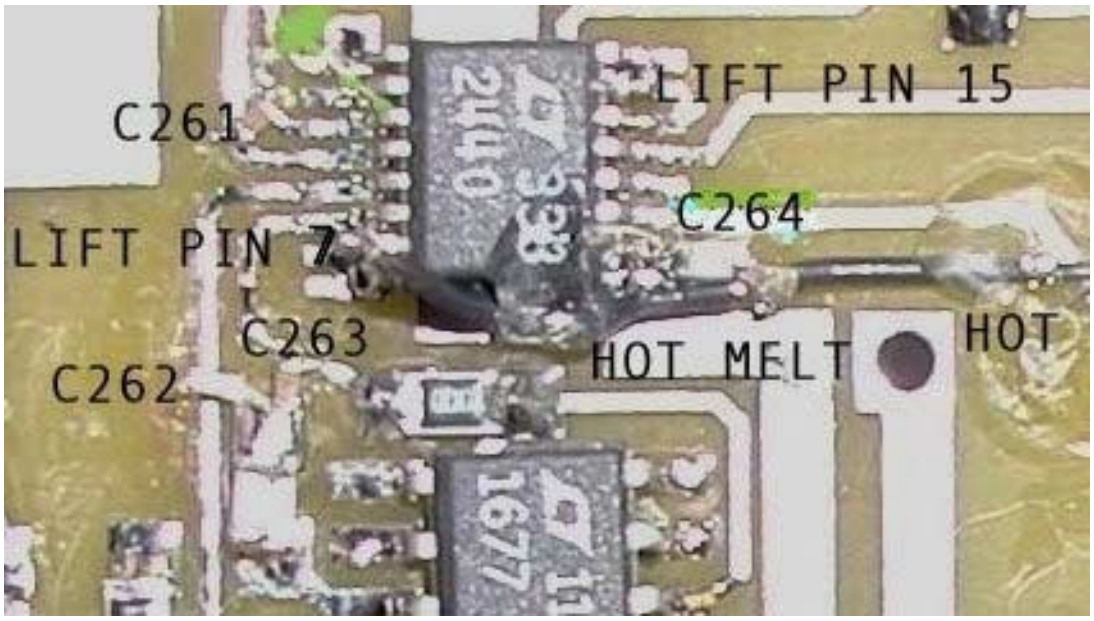
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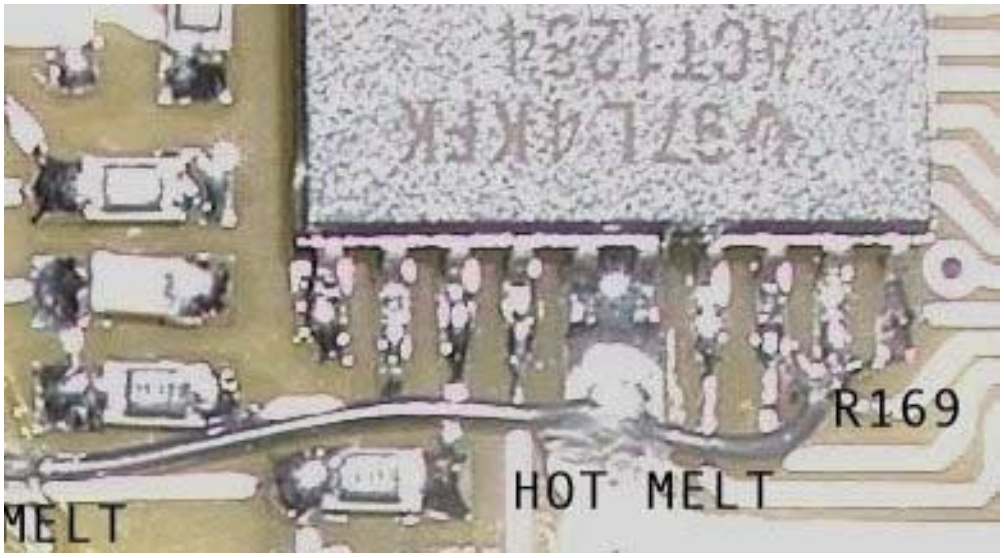
HOT MELT
C262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MELT


C250